Datasheet

G32A1445

Arm® Cortex® -M4F core-based 32-bit MCU

Version: V2.1

1 Product Characteristics

- **Core**
  - 32-bit Arm® Cortex® -M4F core with FPU
  - Up to 112MHz working frequency
- **Memory and interface**
  - Flash with ECC: 512KB
  - SRAM with ECC:64KB
  - 64KB Data Flash with ECC
  - 4KB CFGRAM for use as SRAM or analog EEPROM
- **Clock**
  - HSE: External 4~40MHz crystal oscillator
  - HSI: Internal 48MHz RC oscillator
  - LSI: Internal 8MHz RC oscillator
  - LPO: Internal 128 kHz low-power RC oscillator
  - SYSPLL: Main phase-locked loop up to 112MHz
- **Power supply and power supply management**
  - VDD range: 2.7V~5.5V
  - VDDA range: VDD ~5.5V
  - Power-on/low-power reset (POR/LVR) supported
  - Low-voltage detector (LVD) supported
- **DMA**
  - A 16-channel DMA controller
  - DMA channel multiplexer DMACHM
- **Debugging Interface**
  - JTAG
  - SWD
- **Debugging function**
  - SWJ-DP
  - DWT
  - ITM
- **TPIU**
  - FPB
- **I/O**
  - Up to 89 I/Os
  - All I/O can be mapped to external interrupt vector
- **Communication peripherals**
  - 1×LPI2C interface
  - 3×LPUART
  - 3×LPSPI
  - 3×CAN (all support CAN FD)
  - 1×CFGIO configurable communication interface
- **Analog peripherals**
  - 2×12-bit ADC
  - 1×comparator (built-in 8-bit DAC)
- **Timer**
  - 4×independent 16-bit timer CFGTMR, each offering 8 standard channels
  - 1×16-bit LPTMR with flexible wake-up control
  - 1×32-bit LPITMR with 4-channel
  - 2×Programmable delay unit PDU
  - 1 × RTC, support calendar function, support alarm and regular wake-up from stop/standby mode
- **Safety and Security**
  - Cryptographic Services Engine (CSEc) implements a complete set of encryption capabilities described in the SHE (Secure Hardware Extension) functional specification
  - 128-bit unique device ID

- CRC computing unit
- 1×internal watchdog(WDT)
- 1×external watchdog monitor(EWDT)
- System Memory Protection Unit(MPU)
- ECC on FLASH and SRAM

Chip package

- LQFP48/64/100

Certification Standard

- AEC-Q100
- ASIL_B

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2 Product Information

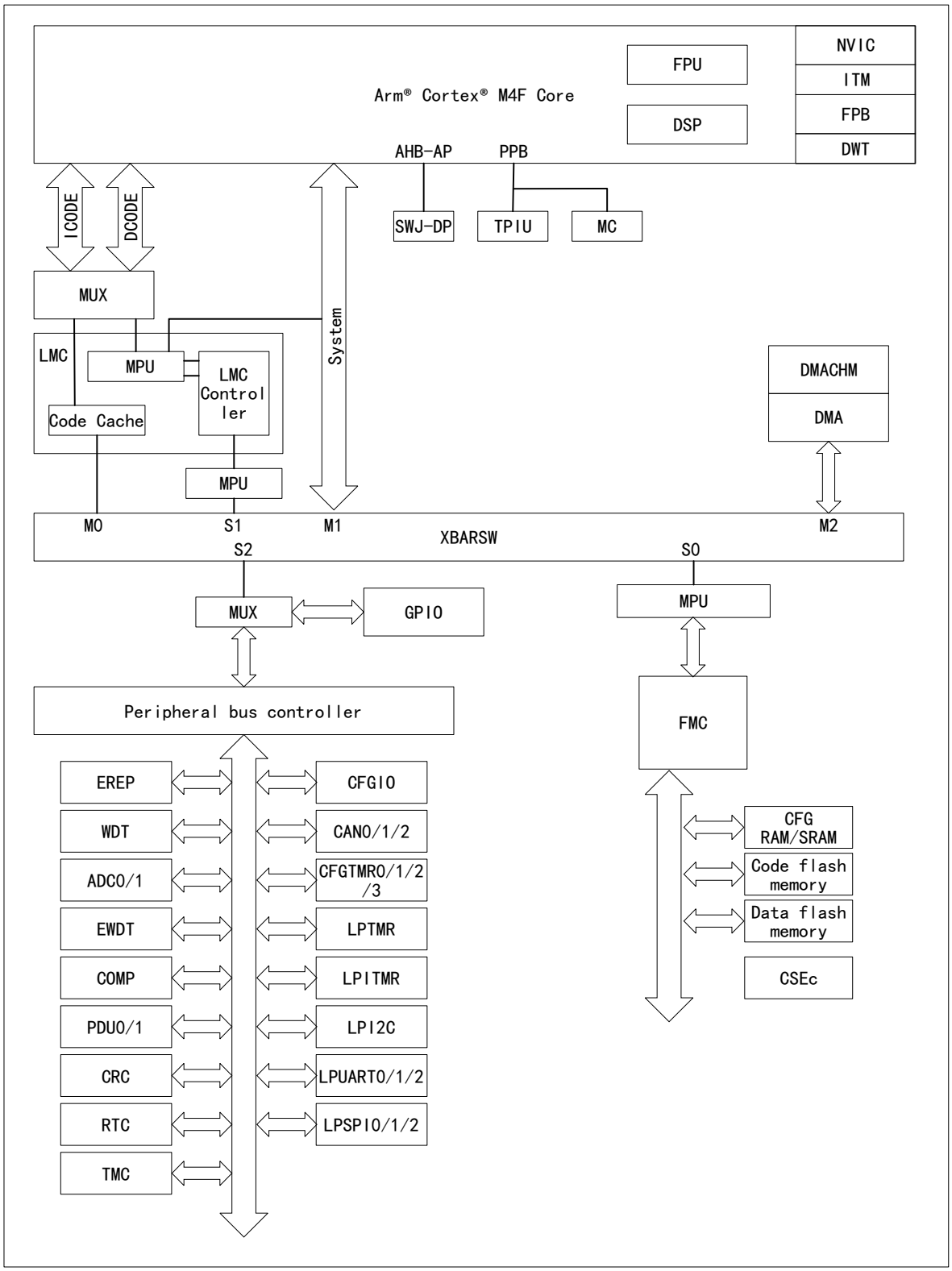
See the following table for G32A1445 product functions and peripheral configuration.

Table 1 Functions and Peripherals of G32A1445 Series Chips

Product		**G32A1445**		
Model		UAT0MLF	UAT0MLH	UAT0MLL
Package		LQFP48	LQFP64	LQFP100
Core		Arm® 32-bit Cortex®-M4F		
Maximum operating frequency (MHz)		112		
Working voltage		2.7-5.5V		
Flash (KB)		512		
SRAM (KB)		64		
GPIOs		43	58	89
Communication interface	LPUART	3		
	LPSPI	3		
	LPI2C	1		
	CAN	3		
	CFGIO	1		
Timer	16-bit CFGTMR	4		
	16-bit LPTMR	1		
	32-bit LPITMR	1		
	WDT	1		
	EWDT	1		
	PDU	2		
Real-time clock		1		
12-bit ADC	Unit	2		
	External channel	14+9	16+13	16+16
Analog comparator||(8-bit DAC)		1(1)		
Operating temperature		Ambient temperature: -40°C to 125°C Junction temperature: -40℃ to 135℃		

3 System Block Diagram

Figure 1 System Block Diagram



4 Pin Configuration and Functions

Figure 2 48-Pin LQFP Top View

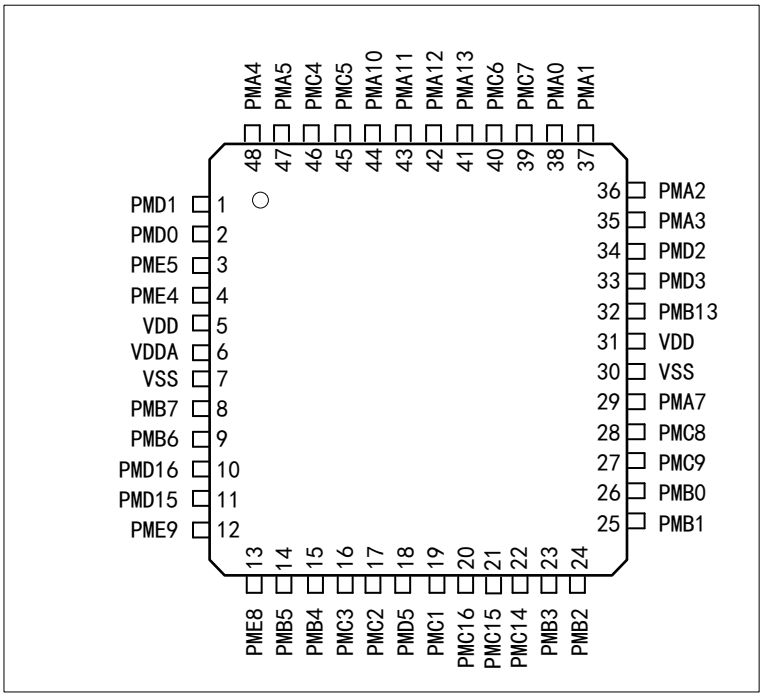


Table 2 Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMA0	38	I/O	Default:ADC0_CH0/COMP0_IN0（ADC0 channel 0/COMP0 input channel 0）
PMA1	37	I/O	Default:ADC0_CH1/COMP0_IN1（ADC0 channel 1/COMP0 input channel 1）
PMA2	36	I/O	Default:ADC1_CH0（ADC1 channel 0）
PMA3	35	I/O	Default:ADC1_CH1（ADC1 channel 1）
PMA4	48	I/O	JTAG_TMS/SWD_DIO
PMA5	47	I/O	RESET_b
PMA7	29	I/O	Default:ADC0_CH3（ADC0 channel 3）
PMA10	44	I/O	JTAG_TDO/noetm_TRACE_SWO
PMA11	43	I/O	GPIO
PMA12	42	I/O	GPIO
PMA13	41	I/O	GPIO
PMB0	26	I/O	Default:ADC0_CH4/ADC1_CH14(ADC0 channel 4/ ADC1 channel 14)

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMB1	25	I/O	Default:ADC0_CH5/ADC1_CH15(ADC0 channel 5/ ADC1 channel 15)
PMB2	24	I/O	Default:ADC0_CH6(ADC0 channel 6)
PMB3	23	I/O	Default:ADC0_CH7(ADC0 channel 7)
PMB4	15	I/O	GPIO
PMB5	14	I/O	GPIO
PMB6	9	I/O	XTAL
PMB7	8	I/O	EXTAL
PMB13	32	I/O	Default:ADC1_CH8/ADC0_CH8(ADC1 channel 8/ADC0 channel 8)
PMC1	19	I/O	Default:ADC0_CH9(ADC0 channel 9)
PMC2	17	I/O	Default:ADC0_CH10/COMP0_IN5(ADC0 channel 10/COMP0 channel 5)
PMC3	16	I/O	Default:ADC0_CH11/COMP0_IN4(ADC0 channel 11/COMP0 channel 4)
PMC4	46	I/O	JTAG_TCLK/SWD_CLK
PMC5	45	I/O	JTAG_TDI
PMC6	40	I/O	Default:ADC1_CH4(ADC1 channel 4)
PMC7	39	I/O	Default:ADC1_CH5(ADC1 channel 5)
PMC8	28	I/O	GPIO
PMC9	27	I/O	GPIO
PMC14	22	I/O	Default:ADC0_CH12(ADC0 channel 12)
PMC15	21	I/O	Default:ADC0_CH13(ADC0 channel 13)
PMC16	20	I/O	Default:ADC0_CH14(ADC0 channel 14)
PMD0	2	I/O	GPIO
PMD1	1	I/O	GPIO
PMD2	34	I/O	Default:ADC1_CH2(ADC1 channel 2)
PMD3	33	I/O	Default:ADC1_CH3(ADC1 channel 3)
PMD5	18	I/O	GPIO
PMD15	11	I/O	GPIO
PMD16	10	I/O	GPIO
PME4	4	I/O	GPIO
PME5	3	I/O	GPIO
PME8	13	I/O	Default:COMP0_IN3(COMP0 channel 3)
PME9	12	I/O	GPIO

PIN		TYPE	DESCRIPTION
NAME	NO.		
VDDA	6	I	Analog voltage,peripheral connection with VDD
VDD	5/31	I	Power supply voltage，peripheral connection
VSS	7/30	G	GND，peripheral connection

Figure 3 64-Pin LQFP Top View

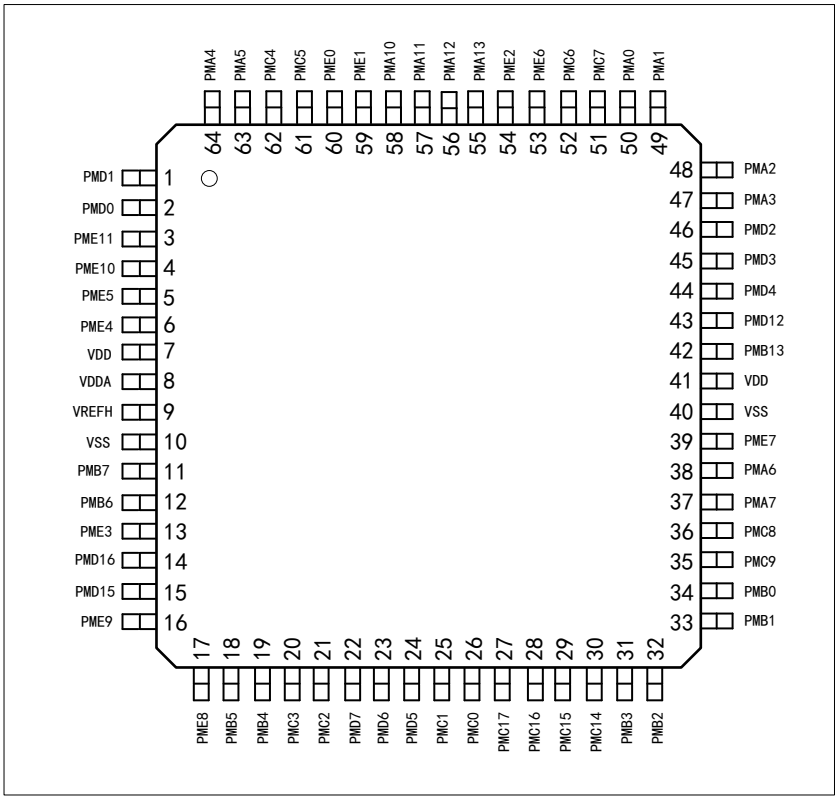


Table 3 Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMA0	50	I/O	Default:ADC0_CH0/COMP0_IN0(ADC0 channel 0/COMP0 input channel 0)
PMA1	49	I/O	Default:ADC0_CH1/COMP0_IN1(ADC0 channel 1/COMP0 input channel 1)
PMA2	48	I/O	Default:ADC1_CH0(ADC1 channel 0)
PMA3	47	I/O	Default:ADC1_CH1(ADC1 channel 1)
PMA4	64	I/O	JTAG_TMS/SWD_DIO
PMA5	63	I/O	RESET_b

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMA6	38	I/O	Default:ADC0_CH2(ADC0 channel 2)
PMA7	37	I/O	Default:ADC0_CH3(ADC0 channel 3)
PMA10	58	I/O	JTAG_TDO/noetm_TRACE_SWO
PMA11	57	I/O	GPIO
PMA12	56	I/O	GPIO
PMA13	55	I/O	GPIO
PMB0	34	I/O	Default:ADC0_CH4/ADC1_CH14(ADC0 channel 4/ ADC1 channel 14)
PMB1	33	I/O	Default:ADC0_CH5/ADC1_CH15(ADC0 channel 5/ ADC1 channel 15)
PMB2	32	I/O	Default:ADC0_CH6(ADC0 channel 6)
PMB3	31	I/O	Default:ADC0_CH7(ADC0 channel 7)
PMB4	19	I/O	GPIO
PMB5	18	I/O	GPIO
PMB6	12	I/O	XTAL
PMB7	11	I/O	EXTAL
PMB12	43	I/O	Default:ADC1_CH7(ADC1 channel 7)
PMB13	42	I/O	Default:ADC1_CH8/ADC0_CH8(ADC1 channel 8/ADC0 channel 8)
PMC0	26	I/O	Default:ADC0_CH8(ADC0 channel 8)
PMC1	25	I/O	Default:ADC0_CH9(ADC0 channel 9)
PMC2	21	I/O	Default:ADC0_CH10/COMP0_IN5(ADC0 channel 10/COMP0 channel 5)
PMC3	20	I/O	Default:ADC0_CH11/COMP0_IN4(ADC0 channel 11/COMP0 channel 4)
PMC4	62	I/O	JTAG_TCLK/SWD_CLK
PMC5	61	I/O	JTAG_TDI
PMC6	52	I/O	Default:ADC1_CH4(ADC1 channel 4)
PMC7	51	I/O	Default:ADC1_CH5(ADC1 channel 5)
PMC8	36	I/O	GPIO
PMC9	35	I/O	GPIO
PMC14	30	I/O	Default:ADC0_CH12(ADC0 channel 12)
PMC15	29	I/O	Default:ADC0_CH13(ADC0 channel 13)
PMC16	28	I/O	Default:ADC0_CH14(ADC0 channel 14)
PMC17	27	I/O	Default:ADC0_CH15(ADC0 channel 15)
PMD0	2	I/O	GPIO

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMD1	1	I/O	GPIO
PMD2	46	I/O	Default:ADC1_CH2(ADC1 channel 2)
PMD3	45	I/O	Default:ADC1_CH3(ADC1 channel 3)
PMD4	44	I/O	Default:ADC1_CH6(ADC1 channel 6)
PMD5	24	I/O	GPIO
PMD6	23	I/O	Default:COMP0_IN7(COMP0 channel 7)
PMD7	22	I/O	Default:COMP0_IN6(COMP0 channel 6)
PMD15	15	I/O	GPIO
PMD16	14	I/O	GPIO
PME0	60	I/O	GPIO
PME1	59	I/O	GPIO
PME2	54	I/O	Default:ADC1_CH10(ADC1 channel 10)
PME3	13	I/O	GPIO
PME4	6	I/O	GPIO
PME5	5	I/O	GPIO
PME6	53	I/O	Default:ADC1_CH11(ADC1 channel 11)
PME7	39	I/O	GPIO
PME8	17	I/O	Default:COMP0_IN3(COMP0 channel 3)
PME9	16	I/O	GPIO
PME10	4	I/O	GPIO
PME11	3	I/O	GPIO
VREFH	9	I	AD Reference Voltage
VDDA	8	I	Analog voltage,peripheral connection with VDD
VDD	7/41	I	Power supply voltage,peripheral connection
VSS	10/40	G	GND,peripheral connection

Figure 4 100-Pin LQFP Top View

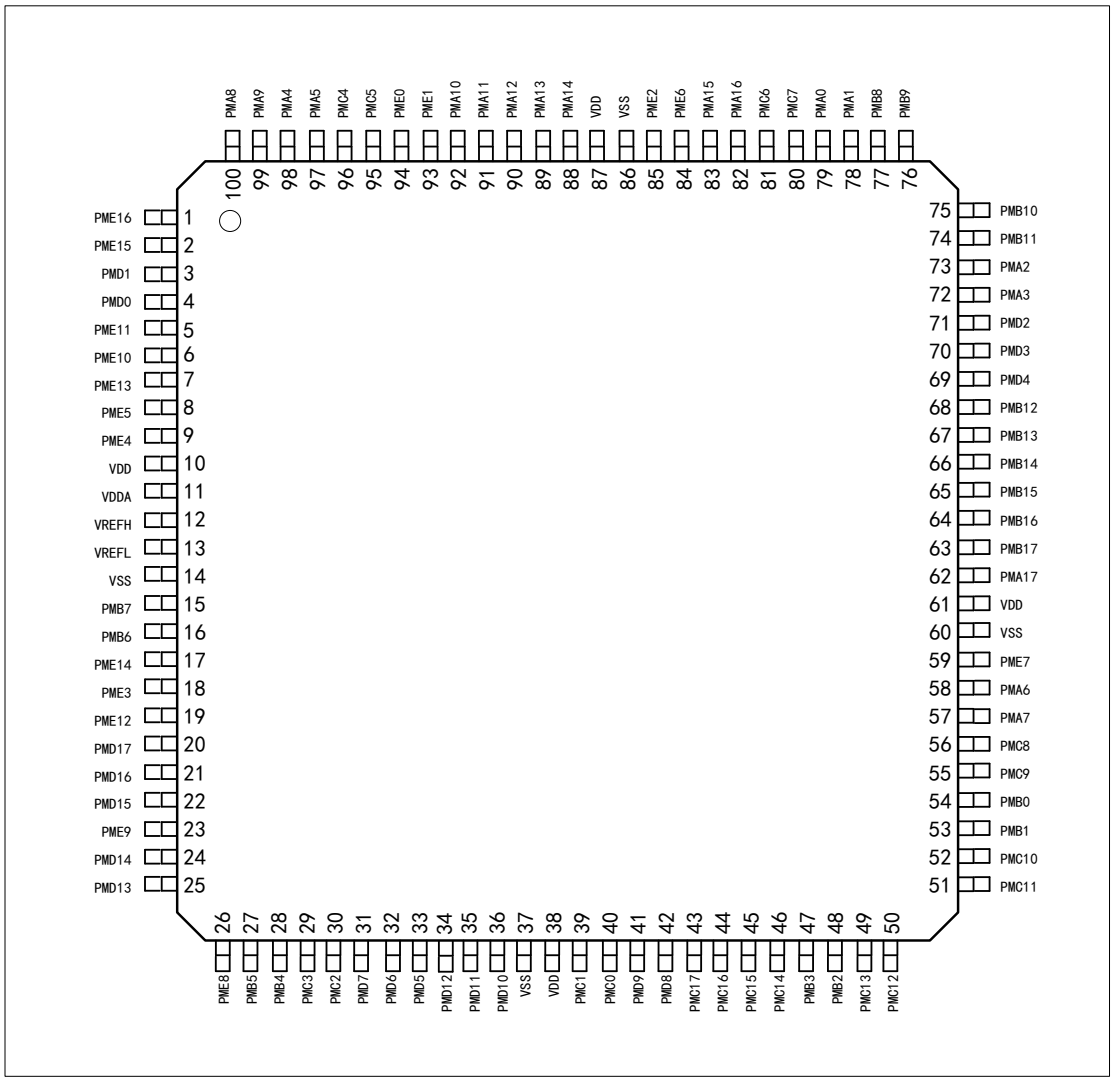


Table 4 Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMA0	79	I/O	Default:ADC0_CH0/COMP0_IN0(ADC0 channel 0/COMP0 input channel 0)
PMA1	78	I/O	Default:ADC0_CH1/COMP0_IN1(ADC0 channel 1/COMP0 input channel 1)
PMA2	73	I/O	Default:ADC1_CH0(ADC1 channel 0)
PMA3	72	I/O	Default:ADC1_CH1(ADC1 channel 1)
PMA4	98	I/O	JTAG_TMS/SWD_DIO
PMA5	97	I/O	RESET_b
PMA6	58	I/O	Default:ADC0_CH2(ADC0 channel 2)
PMA7	57	I/O	Default:ADC0_CH3(ADC0 channel 3)

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMA8	100	I/O	GPIO
PMA9	99	I/O	GPIO
PMA10	92	I/O	JTAG_TDO/noetm_TRACE_SWO
PMA11	91	I/O	GPIO
PMA12	90	I/O	GPIO
PMA13	89	I/O	GPIO
PMA14	88	I/O	GPIO
PMA15	83	I/O	Default:ADC1_CH12(ADC1 channel 12)
PMA16	82	I/O	Default:ADC1_CH13(ADC1 channel 13)
PMA17	62	I/O	GPIO
PMB0	54	I/O	Default:ADC0_CH4/ADC1_CH14(ADC0 channel 4/ ADC1 channel 14)
PMB1	53	I/O	Default:ADC0_CH5/ADC1_CH15(ADC0 channel 5/ ADC1 channel 15)
PMB2	48	I/O	Default:ADC0_CH6(ADC0 channel 6)
PMB3	47	I/O	Default:ADC0_CH7(ADC0 channel 7)
PMB4	28	I/O	GPIO
PMB5	27	I/O	GPIO
PMB6	16	I/O	XTAL
PMB7	15	I/O	EXTAL
PMB8	77	I/O	GPIO
PMB9	76	I/O	GPIO
PMB10	75	I/O	GPIO
PMB11	74	I/O	GPIO
PMB12	68	I/O	Default:ADC1_CH7(ADC1 channel 7)
PMB13	67	I/O	Default:ADC1_CH8/ADC0_CH8(ADC1 channel 8/ADC0 channel 8)
PMB14	66	I/O	Default:ADC1_CH9/ADC0_CH9(ADC1 channel 9/ADC0 channel 9)
PMB15	65	I/O	Default:ADC1_CH14(ADC1 channel 14)
PMB16	64	I/O	Default:ADC1_CH15(ADC1 channel 15)
PMB17	63	I/O	GPIO
PMC0	40	I/O	Default:ADC0_CH8(ADC0 channel 8)
PMC1	39	I/O	Default:ADC0_CH9(ADC0 channel 9)

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMC2	30	I/O	Default:ADC0_CH10/COMP0_IN5(ADC0 channel 10/COMP0 channel 5)
PMC3	29	I/O	Default:ADC0_CH11/COMP0_IN4(ADC0 channel 11/COMP0 channel 4)
PMC4	96	I/O	JTAG_TCLK/SWD_CLK
PMC5	95	I/O	JTAG_TDI
PMC6	81	I/O	Default:ADC1_CH4(ADC1 channel 4)
PMC7	80	I/O	Default:ADC1_CH5(ADC1 channel 5)
PMC8	56	I/O	GPIO
PMC9	55	I/O	GPIO
PMC10	52	I/O	GPIO
PMC11	51	I/O	GPIO
PMC12	50	I/O	GPIO
PMC13	49	I/O	GPIO
PMC14	46	I/O	Default:ADC0_CH12(ADC0 channel 12)
PMC15	45	I/O	Default:ADC0_CH13(ADC0 channel 13)
PMC16	44	I/O	Default:ADC0_CH14(ADC0 channel 14)
PMC17	43	I/O	Default:ADC0_CH15(ADC0 channel 15)
PMD0	4	I/O	GPIO
PMD1	3	I/O	GPIO
PMD2	71	I/O	Default:ADC1_CH2(ADC1 channel 2)
PMD3	70	I/O	Default:ADC1_CH3(ADC1 channel 3)
PMD4	69	I/O	Default:ADC1_CH6(ADC1 channel 6)
PMD5	33	I/O	GPIO
PMD6	32	I/O	Default:COMP0_IN7(COMP0 channel 7)
PMD7	31	I/O	Default:COMP0_IN6(COMP0 channel 6)
PMD8	42	I/O	GPIO
PMD9	41	I/O	GPIO
PMD10	36	I/O	GPIO
PMD11	35	I/O	GPIO
PMD12	34	I/O	GPIO
PMD13	25	I/O	GPIO

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMD14	24	I/O	GPIO
PMD15	22	I/O	GPIO
PMD16	21	I/O	GPIO
PMD17	20	I/O	GPIO
PME0	94	I/O	GPIO
PME1	93	I/O	GPIO
PME2	85	I/O	Default:ADC1_CH10(ADC1 channel 10)
PME3	18	I/O	GPIO
PME4	9	I/O	GPIO
PME5	8	I/O	GPIO
PME6	84	I/O	Default:ADC1_CH11(ADC1 channel 11)
PME7	59	I/O	GPIO
PME8	26	I/O	Default:COMP0_IN3(COMP0 channel 3)
PME9	23	I/O	GPIO
PME10	6	I/O	GPIO
PME11	5	I/O	GPIO
PME12	19	I/O	GPIO
PME13	7	I/O	GPIO
PME14	17	I/O	GPIO
PME15	2	I/O	GPIO
PME16	1	I/O	GPIO
VREFH	12	I	AD Reference Voltage
VDDA	11	I	Analog voltage,peripheral connection with VDD
VDD	10/38/61/87	I	Power supply voltage,peripheral connection
VREFL	13	G	AD Reference GND
VSS	86/60/37/14	G	GND,peripheral connection

5 Pin Multiplexing

Table 5 Pin Multiplexing

G32A1445			GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
LQFP48	LQFP64	LQFP100									
-	-	1	PME16	-	PME16	LPUART1_RTS	LPSPI2_SIN	CFGTMR2_CH7	-	CFGIO_D3	TMC_OUT7
-	-	2	PME15	-	PME15	LPUART1_CTS	LPSPI2_SCK	CFGTMR2_CH6	-	CFGIO_D2	TMC_OUT6
1	1	3	PMD1	-	PMD1	CFGTMR0_CH3	LPSPI1_SIN	CFGTMR2_CH1	-	CFGIO_D1	TMC_OUT2
2	2	4	PMD0	-	PMD0	CFGTMR0_CH2	LPSPI1_SCK	CFGTMR2_CH0	-	CFGIO_D0	TMC_OUT1
-	3	5	PME11	-	PME11	LPSPI2_PCS0	LPTMR0_ALT1	CFGTMR2_CH5	-	CFGIO_D5	TMC_OUT5
-	4	6	PME10	-	PME10	CLKOUT	LPSPI2_PCS1	CFGTMR2_CH4	-	CFGIO_D4	TMC_OUT4
-	-	7	PME13	-	PME13	-	LPSPI2_PCS2	CFGTMR2_FLT0	-	-	-
3	5	8	PME5	-	PME5	TCLK2	CFGTMR2_QD_PHA	CFGTMR2_CH3	CAN0_TX	CFGIO_D7	EWDT_IN
4	6	9	PME4	-	PME4	-	CFGTMR2_QD_PHB	CFGTMR2_CH2	CAN0_RX	CFGIO_D6	EWDT_OUT_b
5	7	10	VDD	VDD	-	-	-	-	-	-	-
6	8	11	VDDA	VDDA	-	-	-	-	-	-	-
-	9	12	VREFH	VREFH	-	-	-	-	-	-	-
-	-	13	VREFL	VREFL	-	-	-	-	-	-	-
7	10	14	VSS	VSS	-	-	-	-	-	-	-
8	11	15	PMB7	EXTAL	PMB7	LPI2C0_SCL	-	-	-	-	-
9	12	16	PMB6	XTAL	PMB6	LPI2C0_SDA	-	-	-	-	-
-	-	17	PME14	-	PME14	CFGTMR0_FLT1	-	CFGTMR2_FLT1	-	-	-

G32A1445			GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
LQFP48	LQFP64	LQFP100									
-	13	18	PME3	-	PME3	CFGTMR0_FLT0	LPUART2_RTS	CFGTMR2_FLT0	-	TMC_IN6	COMP0_OUT
-	-	19	PME12	-	PME12	CFGTMR0_FLT3	LPUART2_TX	-	-	-	-
-	-	20	PMD17	-	PMD17	CFGTMR0_FLT2	LPUART2_RX	-	-	-	-
10	14	21	PMD16	-	PMD16	CFGTMR0_CH1	-	LPSPI0_SIN	COMP0_RRT	-	-
11	15	22	PMD15	-	PMD15	CFGTMR0_CH0	-	LPSPI0_SCK	-	-	-
12	16	23	PME9	-	PME9	CFGTMR0_CH7	LPUART2_CTS	-	-	-	-
-	-	24	PMD14	-	PMD14	CFGTMR2_CH5	LPUART1_TX	-	-	-	CLKOUT
-	-	25	PMD13	-	PMD13	CFGTMR2_CH4	LPUART1_RX	-	-	-	RTC_CLKOUT
13	17	26	PME8	COMP0_IN3	PME8	CFGTMR0_CH6	-	-	-	-	-
14	18	27	PMB5	-	PMB5	CFGTMR0_CH5	LPSPI0_PCS1	LPSPI0_PCS0	CLKOUT	TMC_IN0	-
15	19	28	PMB4	-	PMB4	CFGTMR0_CH4	LPSPI0_SOUT	-	-	TMC_IN1	-
16	20	29	PMC3	ADC0_CH11/COMP0_IN4	PMC3	CFGTMR0_CH3	CAN0_TX	LPUART0_TX	-	-	-
17	21	30	PMC2	ADC0_CH10/COMP0_IN5	PMC2	CFGTMR0_CH2	CAN0_RX	LPUART0_RX	-	-	-
-	22	31	PMD7	COMP0_IN6	PMD7	LPUART2_TX	-	CFGTMR2_FLT3	-	-	-
-	23	32	PMD6	COMP0_IN7	PMD6	LPUART2_RX	-	CFGTMR2_FLT2	-	-	-
18	24	33	PMD5	-	PMD5	CFGTMR2_CH3	LPTMR0_ALT2	CFGTMR2_FLT1	-	TMC_IN7	-
-	-	34	PMD12	-	PMD12	CFGTMR2_CH2	-	-	-	LPUART2_RTS	-
-	-	35	PMD11	-	PMD11	CFGTMR2_CH1	CFGTMR2_QD_PHA	-	-	LPUART2_CTS	-
-	-	36	PMD10	-	PMD10	CFGTMR2_CH0	CFGTMR2_QD_PHB	-	-	-	-
-	40	37	VSS	VSS	-	-	-	-	-	-	-

G32A1445			GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
LQFP48	LQFP64	LQFP100									
-	-	38	VDD	VDD	-	-	-	-	-	-	-
19	25	39	PMC1	ADC0_CH9	PMC1	CFGTMR0_CH1	LPSPI2_SOUT	-	-	CFGTMR1_CH7	-
-	26	40	PMC0	ADC0_CH8	PMC0	CFGTMR0_CH0	LPSPI2_SIN	-	-	CFGTMR1_CH6	-
-	-	41	PMD9	-	PMD9	-	CFGIO_D0	CFGTMR2_FLT3	-	CFGTMR1_CH5	-
-	-	42	PMD8	-	PMD8	-	-	CFGTMR2_FLT2	CFGIO_D1	CFGTMR1_CH4	-
-	27	43	PMC17	ADC0_CH15	PMC17	CFGTMR1_FLT3	CAN2_TX	-	-	-	-
20	28	44	PMC16	ADC0_CH14	PMC16	CFGTMR1_FLT2	CAN2_RX	-	-	-	-
21	29	45	PMC15	ADC0_CH13	PMC15	CFGTMR1_CH3	LPSPI2_SCK	-	-	TMC_IN8	-
22	30	46	PMC14	ADC0_CH12	PMC14	CFGTMR1_CH2	LPSPI2_PCS0	-	-	TMC_IN9	-
23	31	47	PMB3	ADC0_CH7	PMB3	CFGTMR1_CH1	LPSPI0_SIN	CFGTMR1_QD_PHA	-	TMC_IN2	-
24	32	48	PMB2	ADC0_CH6	PMB2	CFGTMR1_CH0	LPSPI0_SCK	CFGTMR1_QD_PHB	-	TMC_IN3	-
-	-	49	PMC13	-	PMC13	CFGTMR3_CH7	CFGTMR2_CH7	LPUART2_RTS	-	-	-
-	-	50	PMC12	-	PMC12	CFGTMR3_CH6	CFGTMR2_CH6	LPUART2_CTS	-	-	-
-	-	51	PMC11	-	PMC11	CFGTMR3_CH5	-	-	-	TMC_IN10	-
-	-	52	PMC10	-	PMC10	CFGTMR3_CH4	-	-	-	TMC_IN11	-
25	33	53	PMB1	ADC0_CH5/ADC1_CH15	PMB1	LPUART0_TX	LPSPI0_SOUT	TCLK0	CAN0_TX	-	-
26	34	54	PMB0	ADC0_CH4/ADC1_CH14	PMB0	LPUART0_RX	LPSPI0_PCS0	LPTMR0_ALT3	CAN0_RX	-	-
27	35	55	PMC9	-	PMC9	LPUART1_TX	CFGTMR1_FLT1	-	-	LPUART0_RTS	-
28	36	56	PMC8	-	PMC8	LPUART1_RX	CFGTMR1_FLT0	-	-	LPUART0_CTS	-
29	37	57	PMA7	ADC0_CH3	PMA7	CFGTMR0_FLT2	-	RTC_CLKIN	-	LPUART1_RTS	-

G32A1445			GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
LQFP48	LQFP64	LQFP100									
-	38	58	PMA6	ADC0_CH2	PMA6	CFGTMR0_FLT1	LPSPI1_PCS1	-	-	LPUART1_CTS	-
-	39	59	PME7	-	PME7	CFGTMR0_CH7	CFGTMR3_FLT0	-	-	-	-
30	-	60	VSS	VSS	-	-	-	-	-	-	-
31	41	61	VDD	VDD	-	-	-	-	-	-	-
-	-	62	PMA17	-	PMA17	CFGTMR0_CH6	CFGTMR3_FLT0	EWDT_OUT_b	-	-	-
-	-	63	PMB17	-	PMB17	CFGTMR0_CH5	LPSPI1_PCS3	-	-	-	-
-	-	64	PMB16	ADC1_CH15	PMB16	CFGTMR0_CH4	LPSPI1_SOUT	-	-	-	-
-	-	65	PMB15	ADC1_CH14	PMB15	CFGTMR0_CH3	LPSPI1_SIN	-	-	-	-
-	-	66	PMB14	ADC1_CH9/ADC0_CH9	PMB14	CFGTMR0_CH2	LPSPI1_SCK	-	-	-	-
32	42	67	PMB13	ADC1_CH8/ADC0_CH8	PMB13	CFGTMR0_CH1	CFGTMR3_FLT1	CAN2_TX	-	-	-
-	43	68	PMB12	ADC1_CH7	PMB12	CFGTMR0_CH0	CFGTMR3_FLT2	CAN2_RX	-	-	-
-	44	69	PMD4	ADC1_CH6	PMD4	CFGTMR0_FLT3	CFGTMR3_FLT3	-	-	-	-
33	45	70	PMD3	ADC1_CH3	PMD3	CFGTMR3_CH5	LPSPI1_PCS0	CFGIO_D5	CFGIO_D7	TMC_IN4	NMI_b
34	46	71	PMD2	ADC1_CH2	PMD2	CFGTMR3_CH4	LPSPI1_SOUT	CFGIO_D4	CFGIO_D6	TMC_IN5	-
35	47	72	PMA3	ADC1_CH1	PMA3	CFGTMR3_CH1	LPI2C0_SCL	EWDT_IN	CFGIO_D5	LPUART0_TX	-
36	48	73	PMA2	ADC1_CH0	PMA2	CFGTMR3_CH0	LPI2C0_SDA	EWDT_OUT_b	CFGIO_D4	LPUART0_RX	-
-	-	74	PMB11	-	PMB11	CFGTMR3_CH3	LPI2C0_HREQ	-	-	-	-
-	-	75	PMB10	-	PMB10	CFGTMR3_CH2	LPI2C0_SDAS	-	-	-	-
-	-	76	PMB9	-	PMB9	CFGTMR3_CH1	LPI2C0_SCLS	-	-	-	-
-	-	77	PMB8	-	PMB8	CFGTMR3_CH0	-	-	-	-	-

G32A1445			GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
LQFP48	LQFP64	LQFP100									
37	49	78	PMA1	ADC0_CH1/COMP0_IN1	PMA1	CFGTMR1_CH1	LPI2C0_SDAS	CFGIO_D3	CFGTMR1_QD_PHA	LPUART0_RTS	TMC_OUT0
38	50	79	PMA0	ADC0_CH0/COMP0_IN0	PMA0	CFGTMR2_CH1	LPI2C0_SCLS	CFGIO_D2	CFGTMR2_QD_PHA	LPUART0_CTS	TMC_OUT3
39	51	80	PMC7	ADC1_CH5	PMC7	LPUART1_TX	CAN1_TX	CFGTMR3_CH3	-	CFGTMR1_QD_PHA	-
40	52	81	PMC6	ADC1_CH4	PMC6	LPUART1_RX	CAN1_RX	CFGTMR3_CH2	-	CFGTMR1_QD_PHB	-
-	-	82	PMA16	ADC1_CH13	PMA16	CFGTMR1_CH3	LPSPI1_PCS2	-	-	-	-
-	-	83	PMA15	ADC1_CH12	PMA15	CFGTMR1_CH2	LPSPI0_PCS3	LPSPI2_PCS3	-	-	-
-	53	84	PME6	ADC1_CH11	PME6	LPSPI0_PCS2	-	CFGTMR3_CH7	-	LPUART1_RTS	-
-	54	85	PME2	ADC1_CH10	PME2	LPSPI0_SOUT	LPTMR0_ALT3	CFGTMR3_CH6	-	LPUART1_CTS	-
-	-	86	VSS	VSS	-	-	-	-	-	-	-
-	-	87	VDD	VDD	-	-	-	-	-	-	-
-	-	88	PMA14	-	PMA14	CFGTMR0_FLT0	CFGTMR3_FLT1	EWDT_IN	-	CFGTMR1_FLT0	-
41	55	89	PMA13	-	PMA13	CFGTMR1_CH7	CAN1_TX	-	-	CFGTMR2_QD_PHA	-
42	56	90	PMA12	-	PMA12	CFGTMR1_CH6	CAN1_RX	-	-	CFGTMR2_QD_PHB	-
43	57	91	PMA11	-	PMA11	CFGTMR1_CH5	-	CFGIO_D1	COMP0_RRT	-	-
44	58	92	PMA10	-	PMA10	CFGTMR1_CH4	-	CFGIO_D0	-	-	JTAG_TDO/noetm_TRACE_SWO
-	59	93	PME1	-	PME1	LPSPI0_SIN	LPI2C0_HREQ	-	LPSPI1_PCS0	CFGTMR1_FLT1	-
-	60	94	PME0	-	PME0	LPSPI0_SCK	TCLK1	-	LPSPI1_SOUT	CFGTMR1_FLT2	-
45	61	95	PMC5	-	PMC5	CFGTMR2_CH0	RTC_CLKOUT	-	-	CFGTMR2_QD_PHB	JTAG_TDI
46	62	96	PMC4	COMP0_IN2	PMC4	CFGTMR1_CH0	RTC_CLKOUT	-	EWDT_IN	CFGTMR1_QD_PHB	JTAG_TCLK/SWD_CLK
47	63	97	PMA5	-	PMA5	-	TCLK1	-	-	-	RESET_b

G32A1445			GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
LQFP48	LQFP64	LQFP100									
48	64	98	PMA4	-	PMA4	-	-	COMP0_OUT	EWDT_OUT_b	-	JTAG_TMS/SWD_DIO
-	-	99	PMA9	-	PMA9	LPUART2_TX	LPSPI2_PCS0	CFGIO_D7	CFGTMR3_FLT2	CFGTMR1_FLT3	-
-	-	100	PMA8	-	PMA8	LPUART2_RX	LPSPI2_SOUT	CFGIO_D6	CFGTMR3_FLT3	-	-

6 Input Multiplexing Priority

Input multiplexing priority is shown in the table below:

Table 6 Input multiplexing priority

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
CAN0_RX	1	0x0000 0011	30	21	17	PMC2
	2	0x0000 0101	9	6	4	PME4
	3	0x0000 0101	54	34	26	PMB0
	4	-	-	-	-	Disable low
CAN1_RX	1	0x0000 0011	81	52	40	PMC6
	2	0x0000 0011	90	56	42	PMA12
	3	-	-	-	-	Disable low
CAN2_RX	1	0x0000 0011	44	28	20	PMC16
	2	0x0000 0100	68	43	-	PMB12
	3	-	-	-	-	Disable low
EWDT_IN	1	0x0000 0100	72	47	35	PMA3
	2	0x0000 0101	96	62	46	PMC4
	3	0x0000 0100	88	-	-	PMA14
	4	0x0000 0111	8	5	3	PME5
	5	-	-	-	-	Disable low
TCLK1	1	0x0000 0011	94	60	-	PME0
	2	0x0000 0011	97	63	47	PMA5
	3	-	-	-	-	Disable low
CFGTMR0_CH0	1	0x0000 0010	68	43	-	PMB12
	2	0x0000 0010	22	15	11	PMD15
	3	0x0000 0010	40	26	-	PMC0
	4	-	-	-	-	Disable low
CFGTMR0_CH1	1	0x0000 0010	39	25	19	PMC1
	2	0x0000 0010	67	42	32	PMB13
	3	0x0000 0010	21	14	10	PMD16
	4	-	-	-	=	Disable low
	1	0x0000 0010	4	2	2	PMD0

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
CFGTMR0_CH2	2	0x0000 0010	30	21	17	PMC2
	3	0x0000 0010	66	-	-	PMB14
	4	-	-	-	-	Disable low
CFGTMR0_CH3	1	0x0000 0010	65	-	-	PMB15
	2	0x0000 0010	3	1	1	PMD1
	3	0x0000 0010	29	20	16	PMC3
	4	-	-	-	-	Disable low
CFGTMR0_CH4	1	0x0000 0010	28	19	15	PMB4
	2	0x0000 0010	64	-	-	PMB16
	3	-	-	-	-	Disable low
CFGTMR0_CH5	1	0x0000 0010	27	18	14	PMB5
	2	0x0000 0010	63	-	-	PMB17
	3	-	-	-	-	Disable low
CFGTMR0_CH6	1	0x0000 0010	26	17	13	PME8
	2	0x0000 0010	62	-	-	PMA17
	3	-	-	-	-	Disable low
CFGTMR0_CH7	1	0x0000 0010	23	16	12	PME9
	2	0x0000 0010	59	39	-	PME7
	3	-	-	-	-	Disable low
CFGTMR0_FLT0	1	0x0000 0010	88	-	-	PMA14
	2	0x0000 0010	18	13	-	PME3
	3	-	-	-	-	Disable low
CFGTMR0_FLT1	1	0x0000 0010	58	38	-	PMA6
	2	0x0000 0010	17	-	-	PME14
	3	-	-	-	-	Disable low
CFGTMR0_FLT2	1	0x0000 0010	57	37	29	PMA7
	2	0x0000 0010	20	-	-	PMD17
	3	-	-	-	-	Disable low
CFGTMR0_FLT3	1	0x0000 0010	69	44	-	PMD4
	2	0x0000 0010	19	-	-	PME12
	3	-	-	-	-	Disable low

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
CFGTMR1_CH0	1	0x0000 0010	48	32	24	PMB2
	2	0x0000 0010	96	62	46	PMC4
	3	-	-	-	-	Disable low
CFGTMR1_CH1	1	0x0000 0010	78	49	37	PMA1
	2	0x0000 0010	47	31	23	PMB3
	3	-	-	-	-	Disable low
CFGTMR1_CH2	1	0x0000 0010	46	30	22	PMC14
	2	0x0000 0010	83	-	-	PMA15
	3	-	-	-	-	Disable low
CFGTMR1_CH3	1	0x0000 0010	45	29	21	PMC15
	2	0x0000 0010	82	-	-	PMA16
	3	-	-	-	-	Disable low
CFGTMR1_CH4	1	0x0000 0110	42	-	-	PMD8
	2	0x0000 0010	92	58	44	PMA10
	3	-	-	-	-	Disable low
CFGTMR1_CH5	1	0x0000 0010	91	57	43	PMA11
	2	0x0000 0110	41	-	-	PMD9
	3	-	-	-	-	Disable low
CFGTMR1_CH6	1	0x0000 0010	90	56	42	PMA12
	2	0x0000 0110	40	26	-	PMC0
	3	-	-	-	-	Disable low
CFGTMR1_CH7	1	0x0000 0110	39	25	19	PMC1
	2	0x0000 0010	89	55	41	PMA13
	3	-	-	-	-	Disable low
CFGTMR1_FLT0	1	0x0000 0110	88	-	-	PMA14
	2	0x0000 0011	56	36	28	PMC8
	3	-	-	-	-	Disable low
CFGTMR1_FLT1	1	0x0000 0110	93	59	-	PME1
	2	0x0000 0011	55	35	27	PMC9
	3	-	-	-	-	Disable low
	1	0x0000 0010	44	28	20	PMC16

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
CFGTMR1_FLT2	2	0x0000 0110	94	60	-	PME0
	3	-	-	-	-	Disable low
CFGTMR1_FLT3	1	0x0000 0110	99	-	-	PMA9
	2	0x0000 0010	43	27	-	PMC17
	3	-	-	-	-	Disable low
CFGTMR1_QD_PHA	1	0x0000 0101	78	49	37	PMA1
	2	0x0000 0100	47	31	23	PMB3
	3	0x0000 0110	80	51	39	PMC7
	4	-	-	-	-	Disable low
CFGTMR1_QD_PHB	1	0x0000 0100	48	32	24	PMB2
	2	0x0000 0110	96	62	46	PMC4
	3	0x0000 0110	81	52	40	PMC6
	4	-	-	-	-	Disable low
CFGTMR2_CH0	1	0x0000 0100	4	2	2	PMD0
	2	0x0000 0010	95	61	45	PMC5
	3	0x0000 0010	36	-	-	PMD10
	4	-	-	-	-	Disable low
CFGTMR2_CH1	1	0x0000 0100	3	1	1	PMD1
	2	0x0000 0010	79	50	38	PMA0
	3	0x0000 0010	35	-	-	PMD11
	4	-	-	-	-	Disable low
CFGTMR2_CH2	1	0x0000 0010	34	-	-	PMD12
	2	0x0000 0100	9	6	4	PME4
	3	-	-	-	-	Disable low
CFGTMR2_CH3	1	0x0000 0100	8	5	3	PME5
	2	0x0000 0010	33	24	18	PMD5
	3	-	-	-	-	Disable low
CFGTMR2_CH4	1	0x0000 0010	25	-	-	PMD13
	2	0x0000 0100	6	4	-	PME10
	3	-	-	-	-	Disable low
	1	0x0000 0010	24	-	-	PMD14

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
CFGTMR2_CH5	2	0x0000 0100	5	3	-	PME11
	3	-	-	-	-	Disable low
CFGTMR2_CH6	1	0x0000 0100	2	-	-	PME15
	2	0x0000 0011	50	-	-	PMC12
	3	-	-	-	-	Disable low
CFGTMR2_CH7	1	0x0000 0011	49	-	-	PMC13
	2	0x0000 0100	1	-	-	PME16
	3	-	-	-	-	Disable low
CFGTMR2_FLT0	1	0x0000 0100	7	-	-	PME13
	2	0x0000 0100	18	13	-	PME3
	3	-	-	-	-	Disable low
CFGTMR2_FLT1	1	0x0000 0100	17	-	-	PME14
	2	0x0000 0100	33	24	18	PMD5
	3	-	-	-	-	Disable low
CFGTMR2_FLT2	1	0x0000 0100	32	23	-	PMD6
	2	0x0000 0100	42	-	-	PMD8
	3	-	-	-	-	Disable low
CFGTMR2_FLT3	1	0x0000 0100	31	22	-	PMD7
	2	0x0000 0100	41	-	-	PMD9
	3	-	-	-	-	Disable low
CFGTMR2_QD_PHA	1	0x0000 0011	8	5	3	PME5
	2	0x0000 0101	79	50	38	PMA0
	3	0x0000 0011	35	-	-	PMD11
	4	0x0000 0110	89	55	41	PMA13
	5	-	-	-	-	Disable low
CFGTMR2_QD_PHB	1	0x0000 0110	95	61	45	PMC5
	2	0x0000 0011	36	-	-	PMD10
	3	0x0000 0011	9	6	4	PME4
	4	0x0000 0110	90	56	42	PMA12
	5	-	-	-	-	Disable low
	1	0x0000 0010	77	-	-	PMB8

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
CFGTMR3_CH0	2	0x0000 0010	73	48	36	PMA2
	3	-	-	-	-	Disable low
CFGTMR3_CH1	1	0x0000 0010	72	47	35	PMA3
	2	0x0000 0010	76	-	-	PMB9
	3	-	-	-	-	Disable low
CFGTMR3_CH2	1	0x0000 0100	81	52	40	PMC6
	2	0x0000 0010	75	-	-	PMB10
	3	-	-	-	-	Disable low
CFGTMR3_CH3	1	0x0000 0010	74	-	-	PMB11
	2	0x0000 0100	80	51	39	PMC7
	3	-	-	-	-	Disable low
CFGTMR3_CH4	1	0x0000 0010	71	46	34	PMD2
	2	0x0000 0010	52	-	-	PMC10
	3	-	-	-	-	Disable low
CFGTMR3_CH5	1	0x0000 0010	51	-	-	PMC11
	2	0x0000 0010	70	45	33	PMD3
	3	-	-	-	-	Disable low
CFGTMR3_CH6	1	0x0000 0100	85	54	-	PME2
	2	0x0000 0010	50	-	-	PMC12
	3	-	-	-	-	Disable low
CFGTMR3_CH7	1	0x0000 0010	49	-	-	PMC13
	2	0x0000 0100	84	53	-	PME6
	3	-	-	-	-	Disable low
CFGTMR3_FLT0	1	0x0000 0011	59	39	-	PME7
	2	0x0000 0011	62	-	-	PMA17
	3	-	-	-	-	Disable low
CFGTMR3_FLT1	1	0x0000 0011	67	42	32	PMB13
	2	0x0000 0011	88	-	-	PMA14
	3	-	-	-	-	Disable low
CFGTMR3_FLT2	1	0x0000 0011	68	43	-	PMB12
	2	0x0000 0101	99	-	-	PMA9

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
	3	-	-	-	-	Disable low
CFGTMR3_FLT3	1	0x0000 0011	69	44	-	PMD4
	2	0x0000 0101	100	-	-	PMA8
	3	-	-	-	-	Disable low
CFGIO_D0	1	0x0000 0110	4	2	2	PMD0
	2	0x0000 0100	92	58	44	PMA10
	3	0x0000 0011	41	-	-	PMD9
	4	-	-	-	-	Disable low
CFGIO_D1	1	0x0000 0110	3	1	1	PMD1
	2	0x0000 0100	91	57	43	PMA11
	3	0x0000 0101	42	-	-	PMD8
	4	-	-	-	-	Disable low
CFGIO_D2	1	0x0000 0110	2	-	-	PME15
	2	0x0000 0100	79	50	38	PMA0
	3	-	-	-	-	Disable low
CFGIO_D3	1	0x0000 0100	78	49	37	PMA1
	2	0x0000 0110	1	-	-	PME16
	3	-	-	-	-	Disable low
CFGIO_D4	1	0x0000 0100	71	46	34	PMD2
	2	0x0000 0110	6	4	-	PME10
	3	0x0000 0101	73	48	36	PMA2
	4	-	-	-	-	Disable low
CFGIO_D5	1	0x0000 0110	5	3	-	PME11
	2	0x0000 0100	70	45	33	PMD3
	3	0x0000 0101	72	47	35	PMA3
	4	-	-	-	-	Disable low
CFGIO_D6	1	0x0000 0110	9	6	4	PME4
	2	0x0000 0100	100	-	-	PMA8
	3	0x0000 0101	71	46	34	PMD2
	4	-	-	-	-	Disable low
CFGIO_D7	1	0x0000 0110	8	5	3	PME5

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
	2	0x0000 0100	99	-	-	PMA9
	3	0x0000 0101	70	45	33	PMD3
	4	-	-	-	-	Disable low
LPI2C0_HREQ	1	0x0000 0011	74	-	-	PMB11
	2	0x0000 0011	93	59	-	PME1
	3	-	-	-	-	Disable low
LPI2C0_SCL	1	0x0000 0011	72	47	35	PMA3
	2	0x0000 0010	15	11	8	PMB7
	3	-	-	-	-	Disable low
LPI2C0_SCLS	1	0x0000 0011	76	-	-	PMB9
	2	0x0000 0011	79	50	38	PMA0
	3	-	-	-	-	Disable low
LPI2C0_SDA	1	0x0000 0010	16	12	9	PMB6
	2	0x0000 0011	73	48	36	PMA2
	3	-	-	-	-	Disable low
LPI2C0_SDAS	1	0x0000 0011	78	49	37	PMA1
	2	0x0000 0011	75	-	-	PMB10
	3	-	-	-	-	Disable low
LPSPI0_PCS0	1	0x0000 0011	54	34	26	PMB0
	2	0x0000 0100	27	18	14	PMB5
	3	-	-	-	-	Disable low
LPSPI0_SCK	1	0x0000 0011	48	32	24	PMB2
	2	0x0000 0010	94	60	-	PME0
	3	0x0000 0100	22	15	11	PMD15
	4	-	-	-	-	Disable low
LPSPI0_SIN	1	0x0000 0010	93	59	-	PME1
	2	0x0000 0011	47	31	23	PMB3
	3	0x0000 0100	21	14	10	PMD16
	4	-	-	-	-	Disable low
LPSPI0_SOUT	1	0x0000 0010	85	54	-	PME2
	2	0x0000 0011	28	19	15	PMB4

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
	3	0x0000 0011	53	33	25	PMB1
	4	-	-	-	-	Disable low
LPSPI1_PCS0	1	0x0000 0011	70	45	33	PMD3
	2	0x0000 0101	93	59	-	PME1
	3	-	-	-	-	Disable low
LPSPI1_SCK	1	0x0000 0011	4	2	2	PMD0
	2	0x0000 0101	66	-	-	PMB14
	3	-	-	-	-	Disable low
LPSPI1_SIN	1	0x0000 0011	65	-	-	PMB15
	2	0x0000 0011	3	1	1	PMD1
	3	-	-	-	-	Disable low
LPSPI1_SOUT	1	0x0000 0011	71	46	34	PMD2
	2	0x0000 0011	64	-	-	PMB16
	3	0x0000 0101	94	60	-	PME0
	4	-	-	-	-	Disable low
LPSPI2_PCS0	1	0x0000 0011	99	-	-	PMA9
	2	0x0000 0011	46	30	22	PMC14
	3	0x0000 0010	5	3	-	PME11
	4	-	-	-	-	Disable low
LPSPI2_SCK	1	0x0000 0011	2	-	-	PME15
	2	0x0000 0011	45	29	21	PMC15
	3	-	-	-	-	Disable low
LPSPI2_SIN	1	0x0000 0011	1	-	-	PME16
	2	0x0000 0011	40	26	-	PMC0
	3	-	-	-	-	Disable low
LPSPI2_SOUT	1	0x0000 0011	100	-	-	PMA8
	2	0x0000 0011	39	25	19	PMC1
	3	-	-	-	-	Disable low
LPTMR0_ALT3	1	0x0000 0011	85	54	-	PME2
	2	0x0000 0100	54	34	26	PMB0
	3	-	-	-	-	Disable low

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
LPUART0_CTS	1	0x0000 0110	56	36	28	PMC8
	2	0x0000 0110	79	50	38	PMA0
	3	-	-	-	-	Disable low
LPUART0_RX	1	0x0000 0110	73	48	36	PMA2
	2	0x0000 0010	54	34	26	PMB0
	3	0x0000 0100	30	21	17	PMC2
	4	-	-	-	-	Disable low
LPUART0_TX	1	0x0000 0110	72	47	35	PMA3
	2	0x0000 0010	53	33	25	PMB1
	3	0x0000 0100	29	20	16	PMC3
	4	-	-	-	-	Disable low
LPUART1_CTS	1	0x0000 0110	58	38	-	PMA6
	2	0x0000 0110	85	54	-	PME2
	3	0x0000 0010	2	-	-	PME15
	4	-	-	-	-	Disable low
LPUART1_RX	1	0x0000 0010	81	52	40	PMC6
	2	0x0000 0010	56	36	28	PMC8
	3	0x0000 0011	25	-	-	PMD13
	4	-	-	-	-	Disable low
LPUART1_TX	1	0x0000 0010	55	35	27	PMC9
	2	0x0000 0010	80	51	39	PMC7
	3	0x0000 0011	24	-	-	PMD14
	4	-	-	-	-	Disable low
LPUART2_CTS	1	0x0000 0011	23	16	12	PME9
	2	0x0000 0110	35	-	-	PMD11
	3	0x0000 0100	50	-	-	PMC12
	4	-	-	-	-	Disable low
LPUART2_RX	1	0x0000 0010	32	23	-	PMD6
	2	0x0000 0011	20	-	-	PMD17
	3	0x0000 0010	100	-	-	PMA8
	4	-	-	-	-	Disable low

Function	Priority	PM_PINCTRLx[MUXCTRL]	Number of 100 Pins	Number of 64 Pins	Number of 48 Pins	Pin
LPUART2_TX	1	0x0000 0010	31	22	-	PMD7
	2	0x0000 0011	19	-	-	PME12
	3	0x0000 0010	99	-	-	PMA9
	4	-	-	-	-	Disable low

7 Electrical Characteristics

7.1 Test under general operating conditions

7.1.1 Absolute maximum rated value

If the load on the device exceeds the absolute maximum rated value, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and it cannot be ensured that the device functions normally under this condition. At the same time, operation shall be performed strictly according to all the conditions defined in the table, and violating any one or more conditions cannot guarantee normal operation of the function.

Unless otherwise specified, all maximum and minimum values can support the full voltage and temperature range.

Table 7 Absolute Maximum Ratings

Symbol	Parameter (1)	Minimum value	Typical value	Maximum value	Unit
T_A(2)	Ambient temperature	-40	-	125	℃
T_{STG}	Storage temperature range	-55	-	165	
I_{INJ}(3)	Continuous DC input current(positive/negative) for injection into I/O pins	-3	-	+3	mA
$\Sigma\|I_{INJ}\|$	Total injection current of all pins (continuous DC limit)	-	-	30	
V_{DD}(4)	2.7V~5.5V input power supply voltage	-0.3	-	5.8(5)	V
V_{REFH}	3.3V/5.0V ADC high reference voltage	-0.3	-	5.8(5)	
V_{IN}	Continuous DC voltage on any I/O pin relative to V_{SS}	-0.8	-	5.8(6)	
$V_{IN\_TRANSIENT}$	Transient overshoot voltage allowed on I/O pins exceeds the V_{IN} limit	-	-	6.8(7)	
T_{ramp_MCU}(8)	MCU supply rise slope	0.5V/min	-	100V/ms	-
T_{ramp}(9)	ECU supply rise slope	0.5V/min	-	500V/ms	-

Notes:

(1) Unless otherwise specified, all voltages are referred to V_{SS} ;

(2) T_J (junction temperature)=135℃. Assuming T_A=125℃ in run mode;
T_J (junction temperature)=125℃. Assuming T_A=105℃ in high-speed run mode;
Assuming the maximum of the 2s2p board is θ JA. Refer to Temperature Characteristics);

(3) When the input pad voltage is close to V_{DD} or V_{SS}, current injection cannot be conducted;

(4) When V_{DD} changes between the minimum and absolute maximum values, both I/O and ADC will change. For detailed information, please refer to the I/O parameters and ADC electrical specifications;

(5) When the lifespan is 60 seconds: unlimited, that is, this part is not held in a reset state and can be switched;

When the service life is 10 hours: this part is held in the reset state through external circuits, and cannot be switched;

When operating with a power supply between 5.5V and 5.8V not in reset state, a total of 60 seconds is allowed, but this part will run with reduced function;

When operating with a power supply between 5.5V and 5.8V while the system is held in the reset state through external circuit, a total of 10 hours is allowed;

All power supplies shall be always maintained within the given working conditions, and once they deviate from the working conditions, the equipment shall be reset or powered off. If the given time or power supply voltage limit is exceeded, permanent damage might be caused to the equipment;

(6) Obey the maximum current injection limit.

(7) Under the condition of 60-second lifespan; the equipment is in a reset state (no output enabled/switched);

(8) The supply rise slope of the electronic control unit (ECU) under typical operating conditions and absolute maximum slope;

(9) The supply rise slope of MCU under typical operating conditions and absolute maximum slope.

7.1.2 Voltage and current operation requirements

The functionality of the equipment is guaranteed above the LVR level, but when the voltage is below 2.7V, the electrical performance of the ADC, COMP, IO, and communication modules will correspondingly decrease.

Table 8 Electrical Characteristics of Voltage and Current [1]

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
V_{DD}[2] [3]	Supply voltage	2.7[4]	-	5.5	V
V_{DDA}[3]	Analog power supply voltage	2.7	-	5.5	
V_{DD} -V_{DDA}[3]	V_{DD}-V_{DDA} voltage difference	-0.1	-	0.1	
V_{ODPU}[5]	Open-drain pull-up voltage	V_{DD}	-	V_{DD}	
$V_{DD(OFF)}$	The voltage allowed to be generated on the VDD pin when the VDD is not powered by any external power supply	0	-	0.1	
I_{INJ}[6]	Injection current of I/O pin (continuous DC)	-3	-	+3	mA
ΣI_{INJ_OP}	The total injection current (continuous DC) of all I/O pins, in order not to reduce the accuracy of the analog module: ADC and ACOMP (refer to	-	-	30	

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
	the "Analog Module" section)				
$V_{REFINTL}$	Low level of ADC built-in reference voltage	-0.1	-	0.1	V
$V_{REFINTH}$(7)	High level of ADC built-in reference voltage	2.7	-	V_{DDA}+0.1	

Notes:

(1) Unless otherwise specified, the data in the table is tested with the typical silicon process under the conditions of T_A=25℃ and V_{DD}=V_{DDA}=V_{REFH}=5V.

(2) The analog characteristics of I/O and ADC will change with the change of V_{DD} between the minimum and maximum values.

(3) VDD and VDDA must be shorted to the common power supply on the PCB. The differential voltage between V_{DD} and V_{DDA} is only used for RF-AC. Select a suitable decoupling capacitor to filter the noise on the power supply.

(4) When executing from internal HSICLK, it will work at 2.7V in all modes

(5) The open-drain output must be pulled to V_{DD}.

(6) When the input pad voltage is close to V_{DD} or V_{SS}, current injection cannot be conducted.

(7) $V_{REFINTH}$ should always be ≤ V_{DDA}+0.1 V and V_{DD}+0.1 V.

7.1.3 Temperature operation characteristics

Table 9 Temperature Operation Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$T_{A(MGP)}$	Ambient temperature under bias conditions	≤80 MHz,RUN mode	-40	-	125	℃
$T_{J(MGP)}$	Junction temperature under bias conditions	≤80 MHz,RUN mode	-40	-	135	
$T_{A(CGP)}$	Ambient temperature under bias conditions	≤112 MHz,HSR mode	-40	-	85	
$T_{J(CGP)}$	Junction temperature under bias conditions	≤112 MHz,HSR mode	-40	-	105	
$T_{A(VGP)}$	Ambient temperature under bias conditions	≤112 MHz,HSR mode	-40	-	105	
$T_{J(VGP)}$	Junction temperature under bias conditions	≤112 MHz,HSR mode	-40	-	125	

7.1.4 Power supply and ground pins

Figure 5 LQFP64 Encapsulation Outgoing Line Separate Decoupling

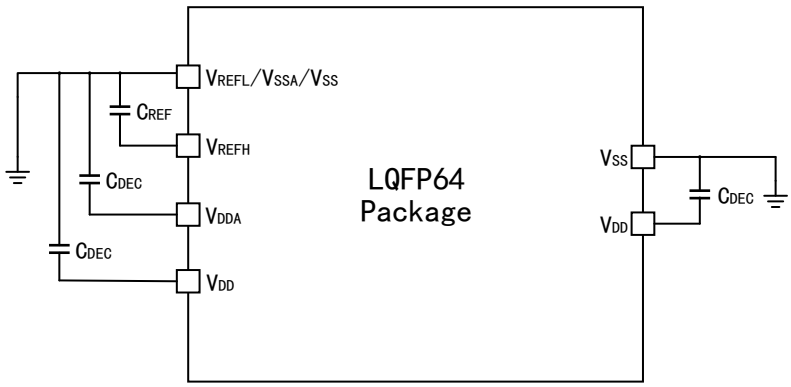
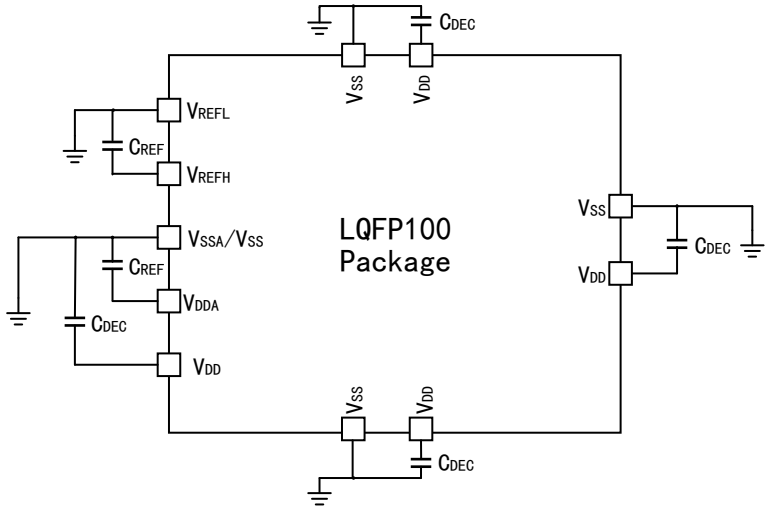


Figure 6 LQFP100 Encapsulation Outgoing Line Separate Decoupling



Note: V_{DD} and V_{DDA} must be shorted to the common power supply on the PCB

Table 10 Decoupling capacitor (1) (2)

Symbol	Parameter	Minimum value(3)	Typical value	Maximum value	Unit
C_{DEC}(4) (6) (7)	Decoupling capacitance	70	100	-	nF
C_{REFINT}(4) (5)	ADC built-in reference high decoupling capacitance	70	100	-	

Notes:

(1) V_{DD} and V_{DDA} must be shorted to the common power supply on the PCB. The differential voltage between V_{DD} and V_{DDA} is only used for RF-AC. Select a suitable decoupling capacitor to filter the noise on the power supply.

(2) All V_{SS} pins should be connected to a PCB-level common ground.

(3) Low-ESR ceramic capacitor (e.g. X7R type) shall be selected as decoupling capacitor.

(4) Recommended minimum value while considering the component aging and tolerance.

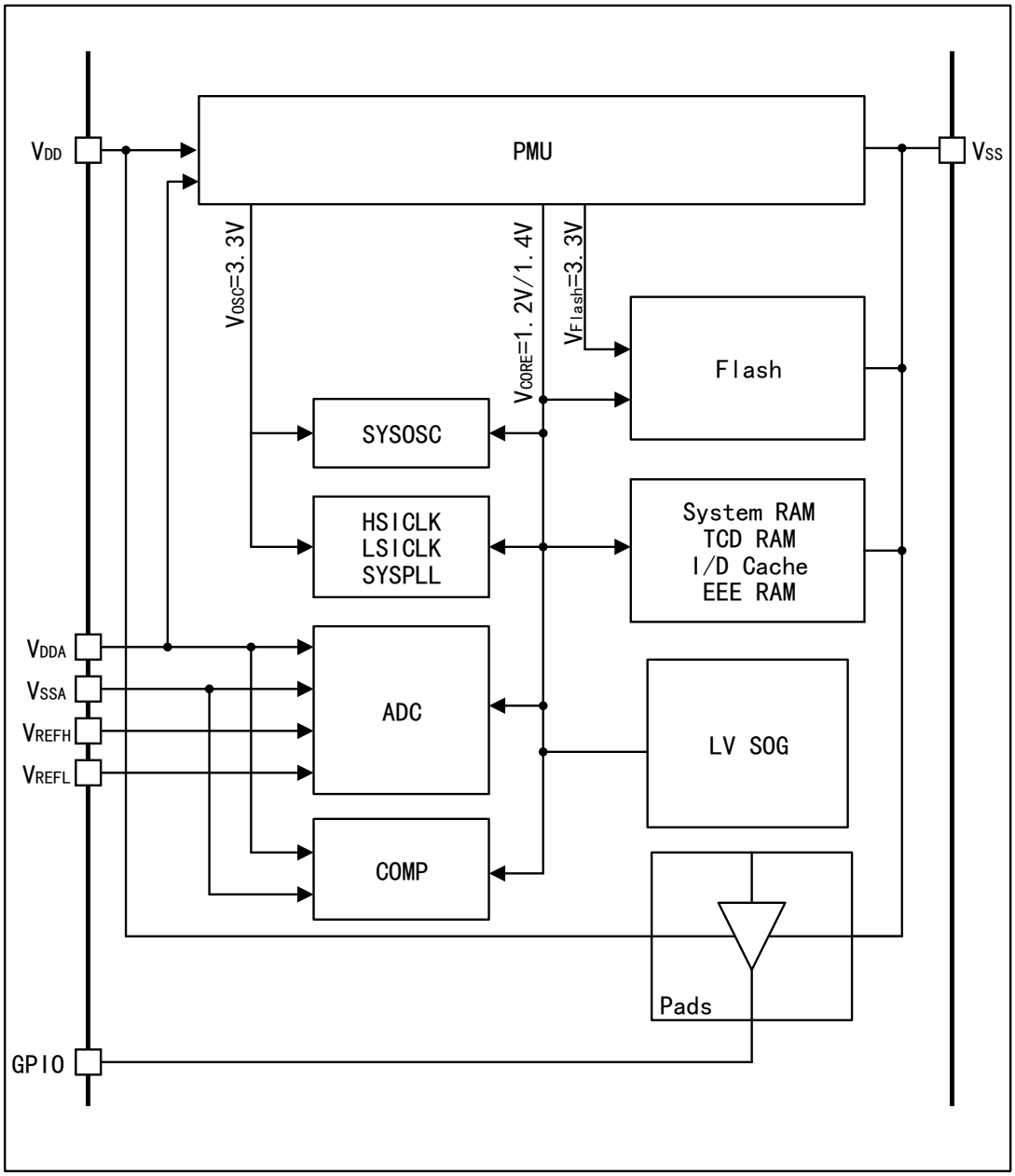
(5) All decoupling capacitors shall be as close as possible to the corresponding power supply and ground pin.

(6) To improve the performance, it is recommended to use 0.1μF, 10μF and 1 nF capacitors in parallel.

(7) The filtering of decoupling device power supply must comply with the following best practice rules:

- The grounding of the protective device and the grounding plane under the integrated circuit shall be connected as short as possible.
- The length of the trace from the protective device to the trace or to the ground shall not exceed 1 mm.
- The protective/decoupling capacitor must be located on the trace path connected to the component.
- The protective/decoupling capacitor must be as close to the input pin of the equipment as possible (at most 2 mm).

Figure 7 Power Supply Scheme



7.1.5 Low-voltage reset and detection system characteristics

Table 11 POR Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
V_{POR}	V_{DD} power-on reset rising and falling detection voltage	1.1	1.6	2.0	V
V_{BG}	Band-gap voltage reference	0.97	1.00	1.03	

Table 12 LVR Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
V_{LVR}	Low-voltage reset falling threshold (RUN, HSR, STOP mode)	2.50	2.58	2.7	V
	Low-voltage reset falling threshold (VLPS/VLPR mode)	1.97	2.22	2.44	
$V_{LVR(HYST)}$ (1)	Low-voltage reset hysteresis (When power-on-voltage is higher than V_{POR})	-	45	-	mV
	Low-voltage reset hysteresis (When power-on-voltage is lower than V_{POR})	-	110	-	

Note: (1) The rising threshold is the sum of falling threshold and hysteresis voltage.

Table 13 LVD Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
V_{LVD}	Low-voltage detection falling threshold	2.8	2.875	3	V
$V_{LVD(HYST)}$ (1)	Low-voltage detection hysteresis	-	50	-	mV

Note: (1) The rising threshold is the sum of falling threshold and hysteresis voltage.

Table 14 LVW Characteristics (1)

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
V_{LVW}	Low-voltage alarm falling threshold	4.19	4.305	4.5	V
$V_{LVW(HYST)}$ (2)	Low-voltage alarm hysteresis	-	75	-	mV

Notes:

(1) When the power supply is working within 3.3 V, as the power supply is less than V_{LVW} all along, it is necessary to always set V_{LVW} (i.e. PMU_LVDCSTS2 [LVWHWINTREN] should remain clear state).

(2) The rising threshold is the sum of falling threshold and hysteresis voltage.

7.1.6 Power mode conversion characteristics

All specifications in the table below use this clock configuration

Table 15 Clock Configuration

Mode	Clock configuration	
RUN mode	Clock Source	HSICLK
	SYS_CLK/CORE_CLK	48MHz
	BUS_CLK	48MHz
	FLASH_CLK	24MHz
HSR mode	Clock Source	SYSPLL

Mode	Clock configuration	
	SYS_CLK/CORE_CLK	112MHz
	BUS_CLK	56MHz
	FLASH_CLK	28MHz
VLPR mode	Clock Source	LSICLK
	SYS_CLK/CORE_CLK	4MHz
	BUS_CLK	4MHz
	FLASH_CLK	1MHz
STOP1/STOP2 mode	Clock Source	HSICLK
	SYS_CLK/CORE_CLK	48MHz
	BUS_CLK	48MHz
	FLASH_CLK	24MHz
VLPS mode	Disable all clock sources (1)	

Note: (1) It refers to HSICLK/SYSOSC/SYSPLL

Table 16 Power Mode Conversion Operation Behavior

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
t_{POR}	The time required to execute the first command from V_{DD} to 2.7V within the operating temperature range of the chip after the power-on reset event occurs.	-	325	-	μs
	RUN→STOP1	0.35	0.38	0.4	μs
	RUN→STOP2	0.2	0.23	0.25	μs
	RUN→VLPS	0.3	0.35	0.4	μs
	RUN→VLPR	3.5	3.8	5	μs
	RUN→Compute operation	0.72	0.75	0.77	μs
	HSR(1) →Compute operation	0.3	0.31	0.35	μs
	VLPS→RUN	8	-	17	μs
	VLPS→VLPR	18.8	23	27.75	μs
	VLPS→Asynchronous DMA Wake-up	105	110	125	μs
	VLPR→VLPS	5.1	5.7	6.5	μs
	VLPR→RUN	19	-	26	μs
	STOP1→RUN	0.07	0.075	0.08	μs
	STOP2→RUN	0.07	0.075	0.08	μs
	STOP1→Asynchronous DMA Wake-up	1	1.1	1.3	μs

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
	STOP2→Asynchronous DMA Wake-up	1	1.1	1.3	μs
	Pin reset→Code execution	-	214	-	μs

Note: (1) HSR mode shall only be used when it is necessary to use frequency exceeding 80 MHz. When using a frequency of 80 MHz and below, it is recommended to use the RUN mode.

7.1.7 Power Consumption

Table 17 Power Consumption (1)

Working mode	Condition	Typical value				Maximum value			Unit
		25℃	85℃	105℃	125℃	85℃	105℃	125℃	
VLPS2)	Disable peripherals (3)	57.5	390.2	787.6	-	599	1408	2174	μA
	Enable LPTMR	63.6	396.6	793.8	-	592	1402	2179	
VLPR	Disable peripherals (4)	1.0	1.5	1.9	-	1.58	2.59	3.54	mA
	Enable peripherals, (situation 1) (4)	1.2	1.5	2.3	-	2.01	2.96	4.91	
	Enable peripherals, (situation 2) (5)	1.3	1.7	2.4	3.6	1.9	2.97	-	
STOP1	-	6.2	6.7	7.4	-	7.07	7.97	9.19	
STOP2	-	6.4	6.9	7.5	-	7.2	8.07	9.35	
RUN	48MHz, disable peripherals	11.8	12.6	13.6	-	16.13	17.79	18.08	
	48MHz, enable peripherals	15.2	15.8	16.9	-	17.24	18.9	19.87	
	64MHz, disable peripherals	17.8	18.5	19.6	-	19.8	20.56	22.63	
	64MHz, enable peripherals	19.6	20	20.9	-	21.29	22.47	24.18	

Working mode	Condition	Typical value				Maximum value			Unit
		25℃	85℃	105℃	125℃	85℃	105℃	125℃	
	80MHz, disable peripherals	15.4	16.2	17.3	-	17.56	19.21	20.1	
	80MHz, enable peripherals	20.3	21.1	22.2	-	21.91	23.18	25.34	
HSR (6)	112MHz, disable peripherals	21.9	22.8	23.9	-	23.45	24.78	-	
	112MHz, enable peripherals	25.2	26.0	27.2	-	26.98	28.27	-	
IDDA/MHz (7)		378	381	390	-	435	445	484	μA/MHz

Notes:

(1) Unless otherwise specified, the data in the table is tested with the typical silicon process under the conditions of T_A=25℃ and V_{DD}=V_{DDA}=$V_{REFINTH}$=5V. These values are only used as indexes of typical silicon processes and user configurations. The actual values may vary due to the differences in silicon distribution and user configuration. All output pins are suspended and the on-chip pull-down resistor is enabled for all unused input pins.

(2) The current data is data based on simplified configuration, which may vary due to the differences in silicon distribution and user configuration.

(3) When PMU_REGCSTS [CLKBDIS] is set to 1. Please refer to the *User Manual* for details.

(4) Data collected by RAM

(5) Limited sample size and data collected by Flash

(6) The maximum ambient temperature for HSR mode is 105℃, and HSR mode shall not be used at 125℃.

(7) The above values are obtained during testing in RUN mode at 80 MHz with the peripheral disabled.

Table 18 Power Consumption of VLPS Additional Cases (1) (2) (3)

Cases	Condition	Typical value (3)				Unit
		25℃	85℃	105℃	125℃	
VLPS and RTC	Clock source: LPO or RTC_CLKIN	58.4	397.3	803.8	1622	μA
VLPS and LPUART wake-up	Clock source: LSICLK Enable address wake-up function	-	-	-	-	

Cases	Condition	Typical value (3)				Unit
		25℃	85℃	105℃	125℃	
	Baud rate: 19.2 kbps					
VLPS and LPUART TX/RX	Clock source: LSICLK Use DMA to transmit or receive data Baud rate: 19.2 kbps	235.8	581.5	988.6	1814.9	
VLPS and LPSPI master mode (4)	Clock source: LSICLK Use DMA to transmit or receive data Baud rate: 500 kHz	1.2	1.7	2.2	3.2	mA
VLPS and LPI2C master mode	Clock source: LSICLK Use DMA to transmit or receive data Baud rate: 100 kHz	1058.8	1487.1	1977.8	2964	
VLPS and LPI2C slave mode wake-up	Clock source: LSICLK Enable address wake-up function Baud rate: 100 kHz	-	-	-	-	μA
VLPS and LPITMR	Clock source: LSICLK Enable one Channel Mode: 32-bit cycle counter	161.3	499	897.3	1702.2	

Notes:

(1) The current data is tested under specific application code and may change due to the changes in user configuration and silicon process.

(2) The power data includes the power caused by periodic wake-up and the operating power of VLPS mode, which will make the power data more dependent on the application code

(3) The typical values are tested based on V_{DD}=V_{DDA}=V_{REFH}=5V, T_A=25℃, and typical silicon process.

(4) The single LPSPI used in G32A1445 refers to LPSPI1.

7.1.8 ESD and Latch-up protection characteristics

Table 19 ESD Electrostatic Discharge Characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model) (1) (2) (3)	-4000	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model) (1) (2) (4)			
	All pins except corner pins	-500	500	V
	Corner pin	-750	750	V

Note: (1) Equipment fault is defined as: "Once the equipment is exposed to ESD pulses, the equipment will not meet the specification requirements."

Table 20 Latch-up Static Latch Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
LU	Latch-up current at T_A=125℃	-100	100	mA

7.1.9 EMC radiated emission characteristics (to be tested)

Geehy can provide EMC measurements that meet IC-level IEC standards as required

7.2 Memory and interface

7.2.1 Time characteristics of Flash command

The following parameters are tested at a clock frequency of FLASHCLK not less than 25MHz.

Table 21 Reading Time Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VB}	Verifying FLASH block is blank time	32KB Flash	-	-	-	ms
		64KB Flash	-	-	0.5	
		128KB Flash	-	-	-	
		256KB Flash	-	-	-	
		512KB Flash	-	-	1.8	
t_{VA}	Verifying FLASH section is blank time	2KB Flash	-	-	75	μs
		4KB Flash	-	-	100	
t_{VAB}	Verifying all FLASH blocks are blank time	-	-	-	2.3	ms
t_{RO}	Read once time	-	-	-	30	μs

Table 22 Programming Time Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{PGCK}	Programming check time	-		-	95	μs
T_{PGDU}	Programming data unit time	-		-	225	μs
t_{PGDA}	Programming data area time	1KB Flash		5	-	ms
t_{PO}	Program once Time	-		125	-	μs

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VBAK}	Verifying backdoor access key time	-		-	35	μs
t_{PGEP}	Programming EEPROM partition time	32KB EEPROM (backup)		70	-	ms
		64KB EEPROM (backup)		71	-	
t_{SFRF}	Set CFGRAM function time	Control code 0xFF		0.09	-	ms
		32KB EEPROM (backup)		0.8	1.2	
		48KB EEPROM (backup)		1	1.5	
		64KB EEPROM (backup)	-	1.3	1.9	
t_{WFRB}	Write CFGRAM in byte time	32KB EEPROM (backup)	-	385	1700	μs
		48KB EEPROM (backup)	-	430	1850	
		64KB EEPROM (backup)	-	475	2000	
t_{WFRHW} (1)	Write CFGRAM in half-word time	32KB EEPROM (backup)	-	385	1700	μs
		48KB EEPROM (backup)	-	430	1850	
		64KB EEPROM (backup)	-	475	2000	
t_{WFRW} (1)	Write CFGRAM in word time	32KB EEPROM (backup)	-	630	2000	μs
		48KB EEPROM (backup)	-	720	2125	
		64KB EEPROM (backup)	-	810	2250	
t_{WEFRW} (1)	Write erased CFGRAM in word time	-	336	-	344	μs
t_{QWW} (1) (2) (3)	Quickly write in word time	First write	-	200	550	μs
		From the second write to the last but one write	-	150	550	
		The last write	-	200	550	

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{QWC}(4)	Quickly write cleanup execution time	-	-	-	2*t_{QWW}	ms

Note:

(1) If the actually displayed time is twice the theoretical value, it may be because after CFGRAM is reset or set, EERAM is written for the first time, causing addition time to clear EEE.

(2) Emulation EEPROM records may be cleared after power down, reset, or completion of a write. If a power-up reset occurs before completion of a write, the last record will be retained and the new record will be cleared. So the data will only be valid after the final write is completed.

(3) The actual maximum value may not be limited to 550us, because additional clearing time may be caused when performing cross-sector operations.

(4) The time required to simulate EEPROM recording. After the last (Nth) write operation is completed, it will automatically complete, assuming it is still powered on at this time. Alternatively, the command can be cleared through SETRAM and executed in the future.

Table 23 Erasing Time Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{EB}	Erase FLASH block time	32KB Flash	-	-	-	ms
		64KB Flash	-	30	550	
		128KB Flash	-	-	-	
		256KB Flash	-	-	-	
		512KB Flash	-	250	4250	
t_{ES}	Erase FLASH sector time	-	-	12	130	ms
t_{EAB}	Erase all blocks time	-	-	400	4900	ms
t_{UEAB}	unsecure erase of all blocks time	-	-	400	4900	ms

Note: (1) Maximum times to erase parameters is based on the expected end of cycle life.

Table 24 Life Time of MTP

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
N_{RW}	Erase cycle	T_A = 125℃	100K	-	-	cycles

7.2.2 Reliability specifications

Table 25 NVM reliability specifications

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
t_{WE16}(1,2)	Write endurance	EEPROM backup to CFGRAM ratio=16	Use as PFlash or DFlash	100K	-	-	writes
t_{WE256}(1)	Write endurance	EEPROM backup to CFGRAM ratio=256		TBD	-	-	writes
t_{DR100}	Data retention	Up to 100% write endurance		TBD	-	-	years
t_{DR10}	Data retention	Up to 100% write endurance		TBD	-	-	years
$t_{DR100KC}$(3)	Data retention	After up to 100K cycles	CFGRAM as emulated EEPROM	10		-	years
t_{CE}(4,5)	Cycling endurance	-		10K	-	-	cycles

Note:

(1) Supported within the full temperature range. Write endurance is specifically used for 32-bit writing to CFGRAM. The larger the ratio, the better the write endurance.

(2) Please refer to the parameters of DFlash for the endurance specifications of emulated EEPROM, except for CFGMemory.

(3) The data retention period per block begins upon the initial user factory programming or after each subsequent erase.

(4) Support programming and erasing of PFlash and DFlash within the full temperature range.

(5) It is per PFlash or DFlash Sector.

7.3 Clock

7.3.1 Characteristics of external clock source

When $G_m > 5*G_{m\_crit}$, the crystal oscillator will stabilize the output clock frequency.

$$G_{m\_crit}=4*(ESR+R_s)*(2\pi f_{osc})^2*(C_0+C_L)^2$$

$$C_L=C_S+[C_{EXTAL}*C_{XTAL}/(C_{EXTAL}+C_{XTAL})]$$

(1) ESR: Equivalent series resistance of external crystal

(2) Rs: A series resistor connecting XTAL pins and external crystals, used to limit current. Users choose appropriate resistance values based on their actual needs to ensure that the oscillation amplitude is appropriate.

(3) f_{osc}: Frequency of external crystal oscillator

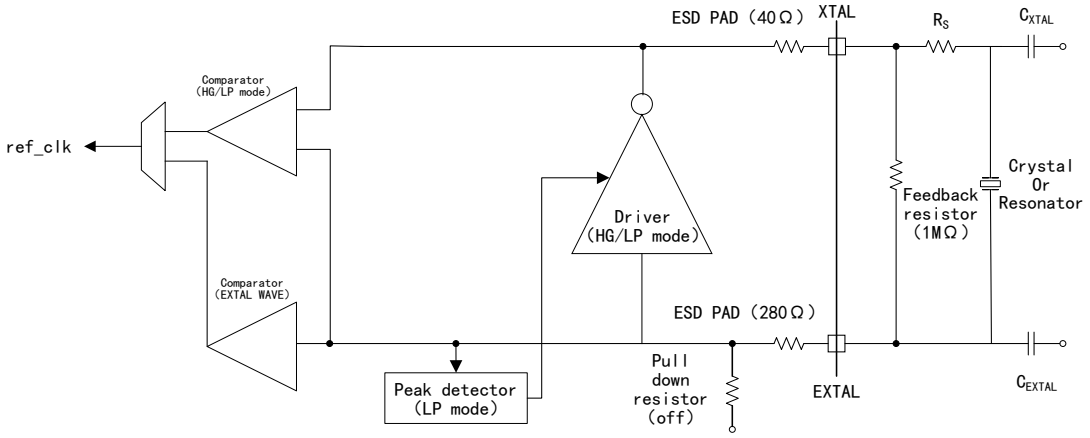
(4) C_0: Shunt capacitance of external crystal oscillator

(5) C_L: Total load capacitance of external crystal oscillator

(6) C_s: Stray or parasitic capacitance on pins caused by any PCB trace

The following diagram shows the circuit diagram of the oscillator connection.

Figure 8 Oscillator connection circuit diagram



The EXTAL and XTAL pins can only be connected to the oscillator components required by the user.

The difference between Low gain mode and High gain mode is that when selecting Low gain mode, internal RF is selected and external RF should not be attached; When selecting the High gain mode, an external resistance of approximately 1M Ω should be used (as shown in the circuit diagram) to ensure the normal operation of the crystal, and the resistance value of the external resistance is allowed to fluctuate by 5%.

Table 26 External Clock Source Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{osc}	Oscillator frequency	-	4	-	40	MHz
f_{in}	Input frequency (1)	External clock mode	-	-	51	MHz

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{in_dc}	Input duty cycle (2)	External clock mode	48	50	55	%
R_F	Feedback resistance	Low-gain mode	-	-	-	MΩ
		High-gain mode	-	1	-	
R_S	Series resistance	Low-gain mode	-	-	-	MΩ
		High-gain mode	-	0	-	
$t_{SU(SYSOSC)}$	Start Time	8MHz Low-gain mode	-	1.5	-	ms
		8MHz High-gain mode	-	2.5	-	ms
		40MHz Low-gain mode	-	2	-	
		40MHz High-gain mode	-	2	-	
G_m	Transconductance of oscillator	SCG_SYSOSCCFG[OSCFSEL]=”10”, namely 4-8MHz	2.2	-	13.7	mA/V
		SCG_SYSOSCCFG[OSCFSEL]=”11”, namely 8-40MHz	11	-	47	mA/V
V_{IL}	input low level	EXTAL pin in external clock mode	V_{SS}	-	1.15	V
V_{IH}	Input high level	EXTAL pin in external clock mode	0.7*V_{DD}	-	V_{DD}	V
C_{EXTAL}	EXTAL pin load capacitance	-	-	-	-	-
C_{XTAL}	XTAL pin load capacitance	-	-	-	-	-
V_{PP_EXTAL}	Peak-to-peak amplitude of oscillation on EXTAL pin	Low-gain mode	1.3	-	-	V
		High-gain mode	2	-	-	V
V_{PP_XTAL}	Peak-to-peak amplitude of oscillation on XTAL pin	Low-gain mode	-	1.0	-	V
		High-gain mode	-	3.3	-	V
$V_{SYSOSCOP}$	Oscillating operating voltage	High-gain mode	0.7	-	-	V

Note:

(1) Frequencies below 40MHz can be used to reduce the duty cycle to 40%~60%. When the frequency is 41MHz~45MHz, a duty cycle of over 40% shall be maintained. When the frequency is 45MHz~50MHz, it is necessary to generate an ADC clock through frequency division.

(2) The duty cycle may have an error of ±5%.

(3) In the actual testing process, in order to avoid the test value of V_{pp_EXTAL} being lower than the actual value, a low capacitance (<5 pF) probe must be used.

7.3.2 Electrical characteristics of system clock generator

7.3.2.1 HSI electrical characteristics

Table 27 HSI Electrical Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HSI}	HSI frequency	-	-	48	-	MHz
Δf_{105}	Frequency Error	Temperature < 105℃	-	0.5	±2	$\%f_{HSI}$
Δf_{125}	Frequency Error	Temperature < 125℃	-	0.5	±2.5	$\%f_{HSI}$
$t_{SU(HSI)}$	Start Time	-	-	3.4	5	μs
T_{ctcj}	Cyclic jitter	HSICLK is used as system clock	-	300	500	ps
T_{1000cj}	Over 1000 cycles of jitter	HSICLK is used as system clock	-	0.04	0.1	$\%f_{HSI}$

Note:

(1) CPK_HP is the CPK in high-performance configuration.

(2) At 25℃, Δf is within 1.5%, center value=48.16MHz, CPK_ HP=1.17

(3) At 125℃, Δf is within 3.3%, center value=47.6MHz, CPK_ HP=2.25

(4) At -40℃, Δf is within 1.5%, center value=48.4MHz, CPK_ HP=0.65

7.3.2.2 LSI electrical characteristics

Table 28 LSI Electrical Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{LSI}	LSI frequency	-	-	8	-	MHz
Δf_{105}	Frequency Error	Temperature < 105℃	-	-	±7	$\%f_{LSI}$
Δf_{125}	Frequency Error	Temperature < 125℃	-	-	±10	$\%f_{LSI}$
$t_{SU(LSI)}$	Start Time	-	-	15	25	μs

Note:

(1) CPK_HP is the CPK in high-performance configuration; CPK_LP is the CPK in low-power configuration

(2) At 25℃, Δf is within 1.5%, center value=8MHz, CPK_ HP=18.19

(3) At 25℃, Δf is within 1.5%, center value=7.99MHz, CPK_ HP=15.71

(4) At 125℃, Δf is within 3.25%, center value=8.06MHz, CPK_ HP=1.7

(5) At 125℃, Δf is within 3.25%, center value=8.13MHz, CPK_ HP=0.96

(6) At -40℃, Δf is within 6.5%, center value=7.79MHz, CPK_ HP=2.02

(7) At -40℃, Δf is within 6.5%, center value=7.67MHz, CPK_ HP=0.99

7.3.3 Electrical characteristics of low-power oscillators

Table 29 LPO Electrical Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{LPO}	LPO frequency	-	110	128	139	KHz
$t_{SU(LPO)}$	Start Time	-	-	-	20	μs

7.3.4 Electrical characteristics of system PLL

Table 30 Electrical Characteristics of SYSPLL

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{SYSPLL}	SYSPLL frequency range	-	8	-	16	MHz
f_{SYSPLL_IN}	SYSPLL input frequency	-	8	-	40	MHz
f_{SYSPLL_OUT}	SYSPLL output frequency	-	90	-	160	MHz
f_{VCO_OUT}	VCO output frequency	-	180	-	320	MHz
T_{pj}	Period jitter	f_{VCO_OUT}=180MHz	-	120	-	ps
		f_{VCO_OUT}=320MHz	-	75	-	ps
T_{aj}	Over 1μs accumulated jitter	f_{VCO_OUT}=180MHz	-	400	-	ps
		f_{VCO_OUT}=320MHz	-	300	-	ps
t_{LDD}	Lock detection time	-	-	-	$150\times10^{-6}+1075(1/f_{SYSPLL})$	s

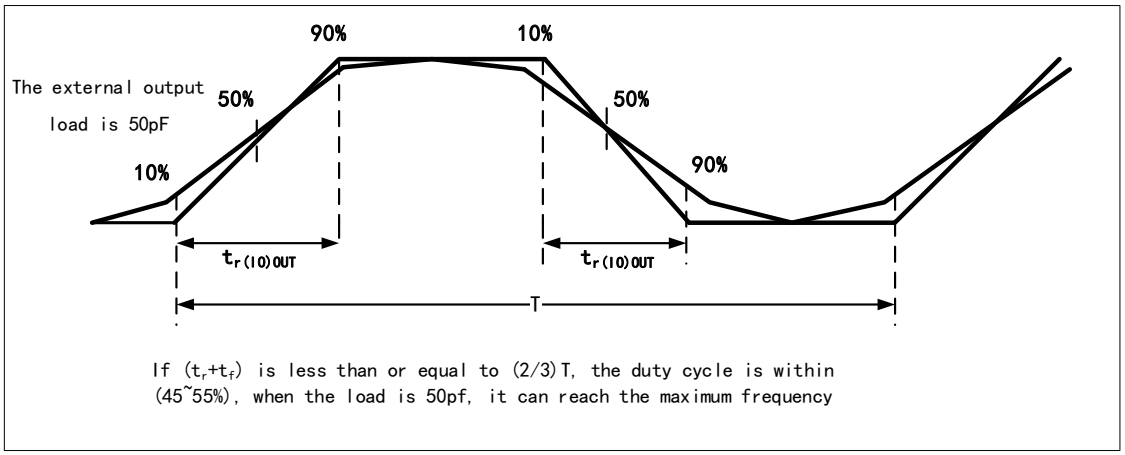
7.4 Clock frequency

The maximum clock output frequency supported by this equipment is 20MHz

7.5 Pin characteristics

7.5.1 AC electrical characteristics

Figure 9 I/O AC Characteristics Definition



7.5.2 General AC specifications

These general specifications apply to all signals configured as GPIO, UART, and timers.

Table 31 General Specifications

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
F_{RST} (1)	Reset input filter pulse	-	-	-	10	ns
NF_{RST} (2)	Reset input unfiltered pulse	-	Max of(100ns,bus clock period)	-	-	ns
- (3) (4)	GPIO pin interrupt pulse width (disable digital fault filter) - synchronous path	-	2	-	-	Bus clock cycle
- (5)	GPIO pin interrupt pulse width (disable digital fault filter, and disable passive filter) - asynchronous path	-	50	-	-	ns

Note:

(1) The maximum length of the RESET pulse that can be filtered by the internal filter only when the passive filter is enabled.

(2) The minimum length of the RESET pulse that can be filtered by the internal filter only when the passive filter is enabled. This number also depends on the bus clock cycle. Then the minimum pulse width that causes reset is 250ns. For faster clock frequencies with clock cycles less than 100ns, the unfiltered minimum pulse width will be 100ns.

(3) The minimum pulse width that ensures passing through the pin synchronous circuit. Short pulse can be recognized when bypassing the synchronizer in stop and VLPS modes, but cannot be recognized in other situations.

(4) The larger values of synchronous and asynchronous timing must be met.

(5) No passive filter is provided at the input end of these pins to ensure the shortest pulse width recognized.

7.5.3 Characteristics of IO port

Table 32 DC Characteristics at 3.3V(T_A=-40℃-105℃, V_{DD}=3.3V)

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
V_{DD}	IO power supply voltage	2.7	3.3	4	V
V_{IL}	Low-level input voltage	V_{SS}-0.3	-	0.3×V_{DD}	V
V_{IH}	High-level input voltage	0.7×V_{DD}	-	V_{DD}+0.3	V
V_{hys}	Input buffer hysteresis	0.06×V_{DD}	-	-	mV
Iol0	I/O current absorption capacity measured when Vol=0.8 V	3	-	-	mA
Ioh0	I/O current source capacity measured when Voh=V_{DD}-0.8V	3.5	-	-	
Iol1	I/O current absorption capacity measured when Vol=0.8 V	10	-	-	
Ioh1	I/O current source capacity measured when Voh=V_{DD}-0.8V	10	-	-	
IOHT	All ports output high current sum	-	-	100	
R_{PU}	Weak pull-up equivalent resistance	20	-	60	kΩ
R_{PD}	Weak pull-down equivalent resistance	20	-	60	kΩ

Table 33 DC Characteristics at 5V (T_A=-40℃-105℃, V_{DD}=5V)

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
V_{DD}	IO power supply voltage	2.7	4	5.5	V
V_{IL}	Low-level input voltage	V_{SS} -0.3	-	0.35×V_{DD}	V
V_{IH}	High-level input voltage	0.7×V_{DD}	-	V_{DD}+0.3	V
V_{hys}	Input buffer hysteresis	0.06×V_{DD}	-	-	mV

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
Iol0	I/O current absorption capacity measured when Vol=0.8 V	5	-	-	mA
Ioh0	I/O current source capacity measured when Voh=V_{DD}-0.8V	5	-	-	
Iol1	I/O current absorption capacity measured when Vol=0.8 V	20	-	-	
Ioh1	I/O current source capacity measured when Voh=V_{DD}-0.8V	20	-	-	
IOHT	All ports output high current sum	-	-	100	
R_{PU}	Weak pull-up equivalent resistance	20	-	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	20	-	50	kΩ

Table 34 AC Characteristics (T_A=25℃)

-	Symbol	Parameter	Condition	3.3V		5V		Unit
				Minimum value	Maximum value	Minimum value	Maximum value	
NA	$t_{f(IO)out}$	Output fall time from high to low level	C_L=25pF	6	14	4	9.6	ns
	$t_{r(IO)out}$	Output rise time from low to high level		7	13	7	10.4	
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=50pF	6	14	4	9.6	
	$t_{r(IO)out}$	Output rise time from low to high level		15	20	15	16	
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=200pF	36	46	22.8	46	
	$t_{r(IO)out}$	Output rise time from low to high level		33	56	22.8	43	
0 (GPIO-HD)	$t_{f(IO)out}$	Output fall time from high to low level	C_L=25pF	6	14	4	9.6	
	$t_{r(IO)out}$	Output rise time from low to high level		7	13	7	10.4	
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=50pF	6	14	4	9.6	
	$t_{r(IO)out}$	Output rise time from low to high level		15	20	15	16	
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=200pF	36	46	22.8	46	

-	Symbol	Parameter	Condition	3.3V		5V		Unit
				Minimum value	Maximum value	Minimum value	Maximum value	
	$t_{r(IO)out}$	Output rise time from low to high level		33	56	22.8	43	
1 (GPIO-HD)	$t_{f(IO)out}$	Output fall time from high to low level	C_L=25pF	4	6	3	6	
	$t_{r(IO)out}$	Output rise time from low to high level		5	7	3.6	6	
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=50pF	6	8	5	6	
	$t_{r(IO)out}$	Output rise time from low to high level		5	8	4	5	
	$t_{f(IO)out}$	Output fall time from high to low level	C_L=200pF	18	22	5	7	
	$t_{r(IO)out}$	Output rise time from low to high level		20	23	5	8	

7.6 Communication peripherals

7.6.1 Electrical characteristics of LPUART

For information about the characteristics of LPUART, please refer to General AC specifications section.

7.6.1.1 Baud rate

Baud rate=Baud clock/((OSRCFG+1) * BRMD).

For information about baud rate, please refer to the description of "Baud Rate " in the *User Manual*.

7.6.2 Electrical characteristics of LPSPI

1. The Low-Power Serial Peripheral Interface (LPSPI) provides synchronous serial bus, and performs master operations and slave operations. Many transmission properties are programmable.
2. The maximum output load for all measurements is 50pF, the input conversion time is 1ns, and the solder pad is configured with the fastest rotation setting (DSCFG=1).
3. All time data in electrical characteristics of LPSP is related to 20% V_{DD} and 80% V_{DD} thresholds.

7.6.2.1 Electrical characteristics of LPSPI run mode

Table 35 Electrical Characteristics of LPSPI Run Mode(1)

Symbol	Parameter	Condition	Run mode (2)						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_P	Peripheral Clock Frequency (3)	Master Mode	-	-	40	-	-	40	MHz
		Slave Mode	-	-	40	-	-	40	
		Main loop (low speed) (4)	-	-	48	-	-	48	
		Main loop (5)	-	-	48	-	-	40	
f_{LPSPI}	Operating Frequency	Master Mode	-	-	10	-	-	10	
		Slave Mode	-	-	10	-	-	10	
		Main loop (low speed) (4)	-	-	12	-	-	12	
		Main loop (5)	-	-	12	-	-	20	
t_{SPSCK}	SPSCK cycle	Master Mode	100	-	-	100	-	-	ns
		Slave Mode	100	-	-	100	-	-	
		Main loop (low speed) (4)	83	-	-	83	-	-	
		Main loop (5)	83	-	-	50	-	-	
t_{hyst}(6)	Enable delay time after	Slave Mode	-	-	-	-	-	-	ns
		Master Mode	(SPDCFG+1)*t_P-25	-	-	(SPDCFG+1)*t_P-25	-	-	

Symbol	Parameter	Condition	Run mode (2)						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
	SPSCK delay	Main loop (low speed) (4)							
		Main loop (5)							
t_{LEAD}(7)	Enable lead time, PCS to SPSCK delay	Slave Mode	-	-	-	-	-	-	ns
		Master Mode	(PSDCFG+1)*t_p-25	-	-	(PSDCFG+1)*t_p-25	-	-	
		Main loop (low speed) (4)							
		Main loop (5)							
t_{WSPSCK} (8)	Time of high SPSCK clock or low SPSCK clock	Master Mode	t_{spsck}/2-3	-	t_{spsck}/2+3	t_{spsck}/2-3	-	t_{spsck}/2+3	ns
		Slave Mode							
		Main loop (low speed) (4)							
		Main loop (5)							
t_{ac}	Slave access time	Slave Mode	-	-	50	-	-	50	ns
t_{dis}	Slave MISO (SOUT) disable time	Slave Mode	-	-	50	-	-	50	ns
$t_{su(in)}$	Data input setup time	Master Mode	38	-	-	29	-	-	ns
		Slave Mode	5	-	-	3	-	-	

Symbol	Parameter	Condition	Run mode (2)						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
		Main loop (low speed) (4)	10	-	-	8	-	-	
		Main loop (5)	8	-	-	7	-	-	
$t_{h(in)}$	Data input hold time	Master Mode	0	-	-	0	-	-	ns
		Slave Mode	3	-	-	3	-	-	
		Main loop (low speed) (4)	3	-	-	3	-	-	
		Main loop (5)	3	-	-	3	-	-	
$t_{h(out)}$	Data output hold time	Master Mode	22	-	-	15	-	-	ns
		Slave Mode	4	-	-	4	-	-	
		Main loop (low speed) (4)	22	-	-	22	-	-	
		Main loop (5)	14	-	-	10	-	-	
t_v	Data validity time after SPSCK edge	Master Mode	-	-	16	-	-	12	ns
		Slave Mode	-	-	39	-	-	30	
		Main loop (low speed) (4)	-	-	10	-	-	8	
		Main loop (5)	-	-	16	-	-	12	
$t_{r(in)}$ $t_{f(in)}$	Data input rise	Master Mode	-	-	12	-	-	12	ns

Symbol	Parameter	Condition	Run mode (2)						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
	and fall time	Slave Mode							
		Main loop (low speed) (4)							
		Main loop (5)							
$t_{r(out)}$ $t_{f(out)}$	Data output rise and fall time	Master Mode	-	-	25	-	-	25	ns
		Slave Mode							
		Main loop (low speed) (4)							
		Main loop (5)							

Notes:

(1) When enabling the main loop mode, the trace length of the SCK pad shall be less than or equal to 11 inches.

(2) When switching from HSR mode to RUN mode, the output clock of LPSPI shall be less than or equal to 14MHz.

(3) f_P= LPSPI peripheral clock, $t_P=1/f_P$.

(4) Main loop mode (low speed): The same as the configuration and function of main loop mode in (5), only applicable to LPSPI0, and the difference is, at low speed, the clock pad PMB2 is used.

(5) Main loop mode: In this mode, set LPSPI_CFGR1[SAMPLE] to 1, and enable LPSPI_SCK clock delay for sampling input data, only applicable to LPSPI0. The clock pads used are PMD15 and PME0.

(6) The baud rate clock of LPSPI is delayed for at least 1 cycle. Set SPDCFG to 0, and the range of SPDCFG is 0~255.

(7) The baud rate clock of LPSPI is delayed for at least 1 cycle. Set PSDCFG to 0, and the range of PSDCFG is 0~255.

(8) When selecting an odd number frequency divider, ensure that the duty cycle conforms to this parameter.

7.6.2.2 Electrical characteristics of LPSPI high-speed run mode

Table 36 Electrical Characteristics of LPSPI High-speed Run Mode (1)

Symbol	Parameter	Condition	High-speed run mode (2)						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_P	Peripheral Clock Frequency (3)	Master Mode	-	-	56	-	-	56	MHz
		Slave Mode	-	-	56	-	-	56	
		Main loop (low speed) (4)	-	-	48	-	-	48	
		Main loop (5)	-	-	48	-	-	48	
f_{LPSPI}	Operating Frequency	Master Mode	-	-	14(6)	-	-	14	
		Slave Mode	-	-	14(6)	-	-	14	
		Main loop (low speed) (4)	-	-	12	-	-	12	
		Main loop (5)	-	-	12	-	-	24	
t_{SPSCK}	SPSCK cycle	Master Mode	72	-	-	72	-	-	ns
		Slave Mode	72	-	-	72	-	-	
		Main loop (low speed) (4)	83	-	-	83	-	-	
		Main loop (5)	83	-	-	42	-	-	
t_{hyst}(7)	Enable delay time	Slave Mode	-	-	-	-	-	-	ns

Symbol	Parameter	Condition	High-speed run mode (2)						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
	after SPSCK delay	Master Mode	(SPDCFG+1)*t_P-25	-	-	(SPDCFG+1)*t_P-25	-	-	
		Main loop (low speed) (4)							
		Main loop (5)							
t_{LEAD}(8)	Enable lead time, PCS to SPSCK delay	Slave Mode	-	-	-	-	-	-	ns
		Master Mode	(PSDCFG+1)*t_p-25	-	-	(PSDCFG+1)*t_p-25	-	-	
		Main loop (low speed) (4)							
		Main loop (5)							
t_{WSPSCK} (9)	Time of high SPSCK clock or low SPSCK clock	Master Mode	t_{spsck}/2-3	-	t_{spsck}/2+3	t_{spsck}/2-3	-	t_{spsck}/2+3	ns
		Slave Mode							
		Main loop (low speed) (4)							
		Main loop (5)							
t_{ac}	Slave access time	Slave Mode	-	-	50	-	-	50	ns
t_{dis}	Slave MISO(SOUT) disable time	Slave Mode	-	-	50	-	-	50	ns

Symbol	Parameter	Condition	High-speed run mode (2)						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
$t_{su(in)}$	Data input setup time	Master Mode	37(10)	-	-	26	-	-	ns
		Slave Mode	5	-	-	3	-	-	
		Main loop (low speed) (4)	9	-	-	7	-	-	
		Main loop (5)	7	-	-	5	-	-	
$t_{h(in)}$	Data input hold time	Master Mode	0	-	-	0	-	-	ns
		Slave Mode	3	-	-	3	-	-	
		Main loop (low speed) (4)	3	-	-	3	-	-	
		Main loop (5)	3	-	-	2	-	-	
$t_{h(out)}$	Data output hold time	Master Mode	23	-	-	15	-	-	ns
		Slave Mode	4	-	-	4	-	-	
		Main loop (low speed) (4)	22	-	-	15	-	-	
		Main loop (5)	14	-	-	10	-	-	
t_v	Data validity time after	Master Mode	-	-	15	-	-	11	ns
		Slave Mode	-	-	36(10)	-	-	26	

Symbol	Parameter	Condition	High-speed run mode (2)						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
	SPSCK edge	Main loop (low speed) (4)	-	-	9	-	-	7	
		Main loop (5)	-	-	15	-	-	11	
$t_{r(in)}$ $t_{f(in)}$	Data input rise and fall time	Master Mode	-	-	9	-	-	9	ns
		Slave Mode							
		Main loop (low speed) (4)							
		Main loop (5)							
$t_{r(out)}$ $t_{f(out)}$	Data output rise and fall time	Master Mode	-	-	25	-	-	25	ns
		Slave Mode							
		Main loop (low speed) (4)							
		Main loop (5)							

Notes:

(1) When enabling the main loop mode, the trace length of the SCK pad shall be less than or equal to 11 inches.

(2) When switching from HSR mode to RUN mode, the output clock of LPSPI shall be less than or equal to 14MHz.

(3) f_P= LPSPI peripheral clock, $t_P=1/f_P$.

(4) Main loop mode (low speed): The same as the configuration and function of main loop mode in (5), only applicable to LPSPI0, and the difference is, at low speed, the clock pad PMB2 is used.

(5) Main loop mode: In this mode, set LPSPI_CFGR1[SAMPLE] to 1, and enable LPSPI_SCK clock delay for sampling input data, only applicable to LPSPI0. The clock pads used are PMD15 and PME0.

(6) Only GPIO-HD PAD type LPSPI0 can achieve the maximum operating frequency f_{LPSPI}. Otherwise, f_{LPSPI}=12Mhz.

(7) The baud rate clock of LPSPI is delayed for at least 1 cycle. Set SPDCFG to 0, and the range of SPDCFG is 0~255.

(8) The baud rate clock of LPSPI is delayed for at least 1 cycle. Set PSDCFG to 0, and the range of PSDCFG is 0~255.

(9) When selecting an odd number frequency divider, ensure that the duty cycle conforms to this parameter.

(10) The maximum operating frequency f_{LPSPI}=12MHz, which has nothing to do with the PAD type and LPSPI instance.

(11) Only applicable to GPIO-HD PAD type LPSPI0, with a maximum operating frequency of f_{LPSPI}=14MHz.

7.6.2.3 Electrical characteristics of LPSPI VLPR mode

Table 37 Electrical Characteristics of LPSPI VLPR Mode (1)

Symbol	Parameter	Condition	VLPR mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_P	Peripheral Clock Frequency (2)	Master Mode	-	-	4	-	-	4	MHz
		Slave Mode	-	-	4	-	-	4	
		Main loop (low speed) (3)	-	-	4	-	-	4	
		Main loop (4)	-	-	4	-	-	4	
f_{LPSPI}	Operating Frequency	Master Mode	-	-	2	-	-	2	
		Slave Mode	-	-	2	-	-	2	
		Main loop (low speed) (3)	-	-	2	-	-	2	

Symbol	Parameter	Condition	VLPR mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
		Main loop (4)	-	-	2	-	-	2	
t_{SPSCK}	SPSCK cycle	Master Mode	500	-	-	500	-	-	ns
		Slave Mode	500	-	-	500	-	-	
		Main loop (low speed) (3)	500	-	-	500	-	-	
		Main loop (4)	500	-	-	500	-	-	
t_{hyst}(6)	Enable delay time after SPSCK delay	Slave Mode	-	-	-	-	-	-	ns
		Master Mode	(SPDCFG+1)*t_p-50	-	-	(SPDCFG+1)*t_p-50	-	-	
		Main loop (low speed) (3)							
		Main loop (4)							
t_{LEAD}(7)	Enable lead time, PCS to SPSCK delay	Slave Mode	-	-	-	-	-	-	ns
		Master Mode	(PSDCFG+1)*t_p-50	-	-	(PSDCFG+1)*t_p-50	-	-	
		Main loop (low speed) (3)							
		Main loop (4)							
t_{WSPSCK} (8)	Time of high SPSCK clock or	Master Mode	t_{spsck}/2-5	-	t_{spsck}/2+5	t_{spsck}/2-5	-	t_{spsck}/2+5	ns
		Slave Mode							

Symbol	Parameter	Condition	VLPR mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
	low SPSCK clock	Main loop (low speed) (3)							
		Main loop (4)							
t_{ac}	Slave access time	Slave Mode	-	-	100	-	-	100	ns
t_{dis}	Slave MISO (SOUT) disable time	Slave Mode	-	-	100	-	-	100	ns
$t_{su(in)}$	Data input setup time	Master Mode	78	-	-	72	-	-	ns
		Slave Mode	18	-	-	18	-	-	
		Main loop (low speed) (3)	20	-	-	20	-	-	
		Main loop (4)	20	-	-	20	-	-	
$t_{h(in)}$	Data input hold time	Master Mode	0	-	-	0	-	-	ns
		Slave Mode	14	-	-	14	-	-	
		Main loop (low speed) (3)	12	-	-	12	-	-	
		Main loop (4)	11	-	-	11	-	-	
$t_{h(out)}$	Data output hold time	Master Mode	29	-	-	22	-	-	ns
		Slave Mode	4	-	-	4	-	-	

Symbol	Parameter	Condition	VLPR mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
		Main loop (low speed) (3)	27	-	-	21	-	-	
		Main loop (4)	19	-	-	14	-	-	
t_v	Data validity time after SPSCK edge	Master Mode	-	-	48	-	-	47	ns
		Slave Mode	-	-	96	-	-	92	
		Main loop (low speed) (3)	-	-	44	-	-	44	
		Main loop (4)	-	-	48	-	-	47	
$t_{r(in)}$ $t_{f(in)}$	Data input rise and fall time	Master Mode	-	-	9	-	-	6	ns
		Slave Mode							
		Main loop (low speed) (3)							
		Main loop (4)							
$t_{r(out)}$ $t_{f(out)}$	Data output rise and fall time	Master Mode	-	-	25	-	-	25	ns
		Slave Mode							
		Main loop (low speed) (3)							
		Main loop (4)							

Notes:

(1) When enabling the main loop mode, the trace length of the SCK pad shall be less than or equal to 11 inches.

(2) f_P= LPSPI peripheral clock, $t_P=1/f_P$.

(3) Main loop mode (low speed): The same as the configuration and function of main loop mode in (4), only applicable to LPSPI0, and the difference is, at low speed, the clock pad PMB2 is used.

(4) Main loop mode: In this mode, set LPSPI_CFGR1[SAMPLE] to 1, and enable LPSPI_SCK clock delay for sampling input data, only applicable to LPSPI0. The clock pads used are PMD15 and PME0.

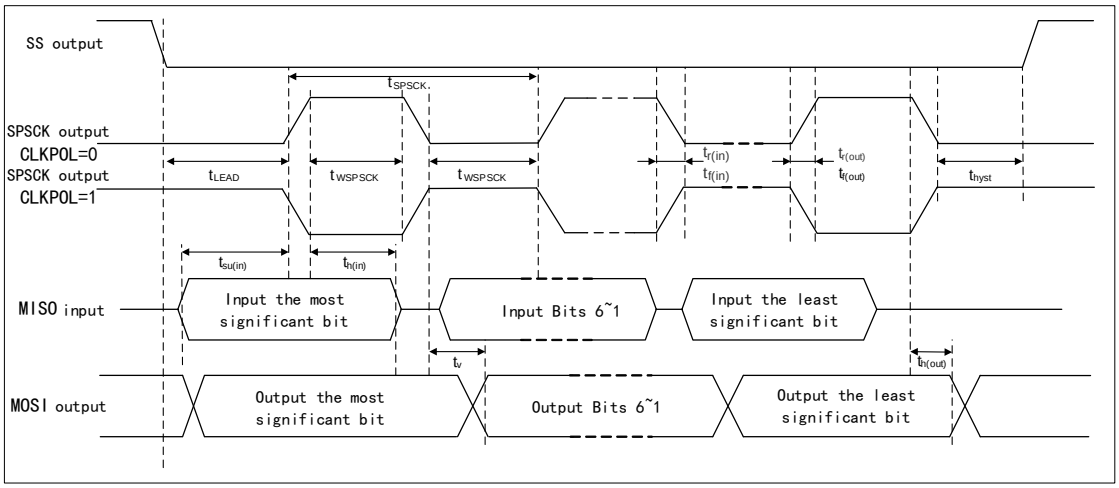
(5) Only GPIO-HD PAD type LPSPI0 can achieve the maximum operating frequency f_{LPSPI}. Otherwise, f_{LPSPI}=12Mhz.

(6) The baud rate clock of LPSPI is delayed for at least 1 cycle. Set SPDCFG to 0, and the range of SPDCFG is 0~255.

(7) The baud rate clock of LPSPI is delayed for at least 1 cycle. Set PSDCFG to 0, and the range of PSDCFG is 0~255.

(8) When selecting an odd number frequency divider, ensure that the duty cycle conforms to this parameter.

Figure 10 LPSPI Main Mode Timing (CLKPHA=0)

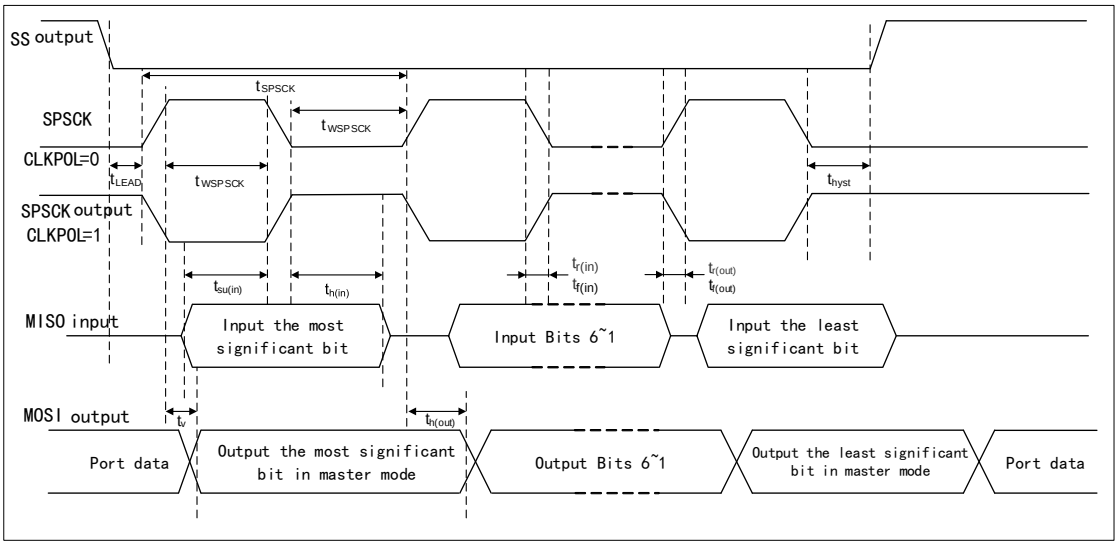


Notes:

(1) When BSEN=0, the input sequence of MISO is MSB, No. 6-1 bits, LSB.

(2) When BSEN=1, the input sequence of MISO is LSB, No. 1-6 bits, MSB.

Figure 11 LPSPI Master Mode Timing (CLKPHA=1)



Notes:

(1) When BSEN=0, the input sequence of MISO is MSB, No. 6-1 bits, LSB.

(2) When BSEN=1, the input sequence of MISO is LSB, No. 1-6 bits, MSB.

Figure 12 LPSPI Slave Mode Timing (CLKPHA=0)

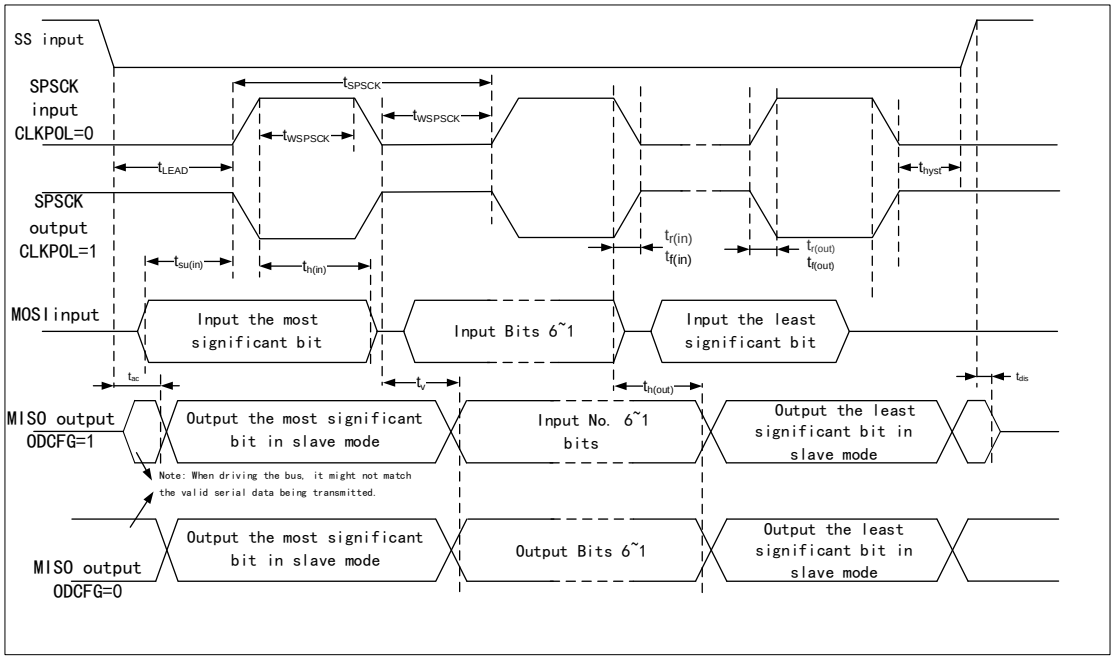
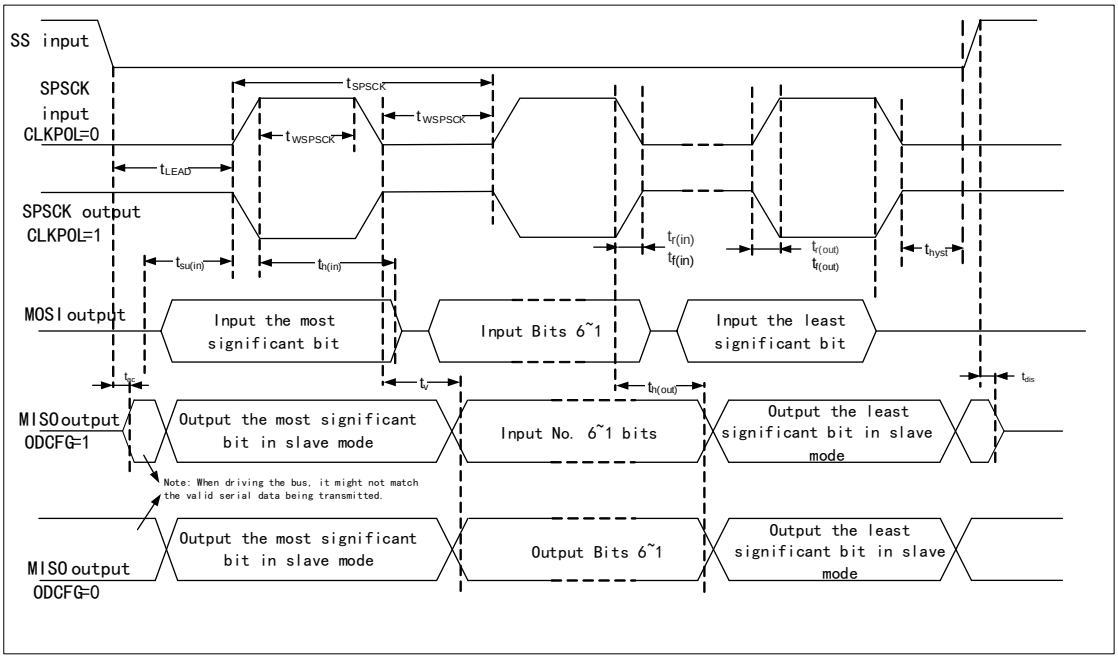


Figure 13 LPSPI Slave Mode Timing (CLKPHA=1)



7.6.3 Electrical characteristics of LPI2C

For information about the characteristics of LPI2C, please refer to General AC specifications section.

For LPI2C configuration information, please refer to the *User Manual*.

7.6.4 Electrical characteristics of CAN

For the bit timing parameters and baud rate required for setting the CAN protocol, please refer to the " Functional differences among different CAN " section of the CAN *User Manual*.

7.7 Analog peripherals

7.7.1 ADC

7.7.1.1 Operating conditions of 12-bit ADC

Table 38 Operating conditions of 12-bit ADC(1)

Symbol	Parameter	Condition	Minimum value	Typical value(2)	Maximum value	Unit
V_{REFH}	High reference voltage(3)	-	Please refer to the "Voltage and Current Operating Requirements " section for relevant data	V_{DDA}	Please refer to the "Voltage and Current Operating Requirements " section for relevant data	V
V_{REFL}	Low reference voltage(3)	-	Please refer to the "Voltage and Current Operating Requirements " section for relevant data	0	Please refer to the "Voltage and Current Operating Requirements " section for relevant data	mV
V_{IN}	ADC input voltage	-	V_{REFL}	-	V_{REFH}	V
f_{ADC}	ADC frequency	Normal use(4-5)	2	40	50	MHz
C_{PIN}	Pin capacitance	-	-	2.1	2.5	pF
C_{ABUS}	Analog bus capacitance	-	-	3	4	

Symbol	Parameter	Condition	Minimum value	Typical value(2)	Maximum value	Unit
C_{ADC}	Sampling capacitance	-	-	5.1(gain=0).. .7.2(gain=max)	6.36(gain=0).. .9.36(gain=max)	
R_{SRC}	Source impedance	f_{ADC}<4MHz	-	-	5	kΩ
R_{CH}	Channel impedance(channel select switch impedance)	-	-	0.650	0.780	
R_{ADC}	Sampling impedance(sampling select switch impedance)	-	-	0.155	1.0	
f_{CONV}	ADC conversion frequency (7-8)	There is no ADC average hardware(6) to enable continuous conversion and subsequent conversion time	46.4	928	1160	Ksps
		Configure the ADC average hardware to 32(6), and enable continuous conversion and subsequent conversion time	1.45	29	36.25	Ksps
	ADC power consumption	-	-	1.0	1.1(9)	mA

Notes:

(1) The data is obtained from a comprehensive evaluation and is not tested in production.

(2) Unless otherwise specified, the parameter conditions of typical values are T_A=25℃, V_{DDA}=5V, f_{ADC}=40MHz, R_{AS}=20Ω and C_{AS}=10nF.

(3) V_{REFH} and V_{REFL} are internally connected to V_{DDA} and V_{SS}. When the reference voltage quality is better than SAR ADC, the maximum performance can be obtained.

(4) Refer to the User Manual to set the clock and comparison cycle.

(5) When the frequency is greater than the maximum frequency of the ADC, the ADC conversion is unstable.

(6) The average template number of hardware can be configured by ADC_CSTS3[HAVGCFG].

(7) This value is tested under the condition of the minimum sampling time of 275ns.

(8) For ADC conversion rate calculation, please refer to the description of “Calibration Function” in *User Manual*.

(9) The test conditions for configuration parameters are:

- V_{DD}=V_{DDA}=V_{REFH}=2.5V-5.5V, T_A=-40℃-135℃
- The bus clock frequency is 48MHz, the ADC time frequency is 48MHz (using HSICLK), the calibration clock is 24MHz, the sampling time is tS=14cyc, and the ADC hardware averaging time is 3212-bit resolution
- Continuous conversion mode
- ADC0_CH1 channel

Figure 14 ADC Input Impedance Equivalent Diagram

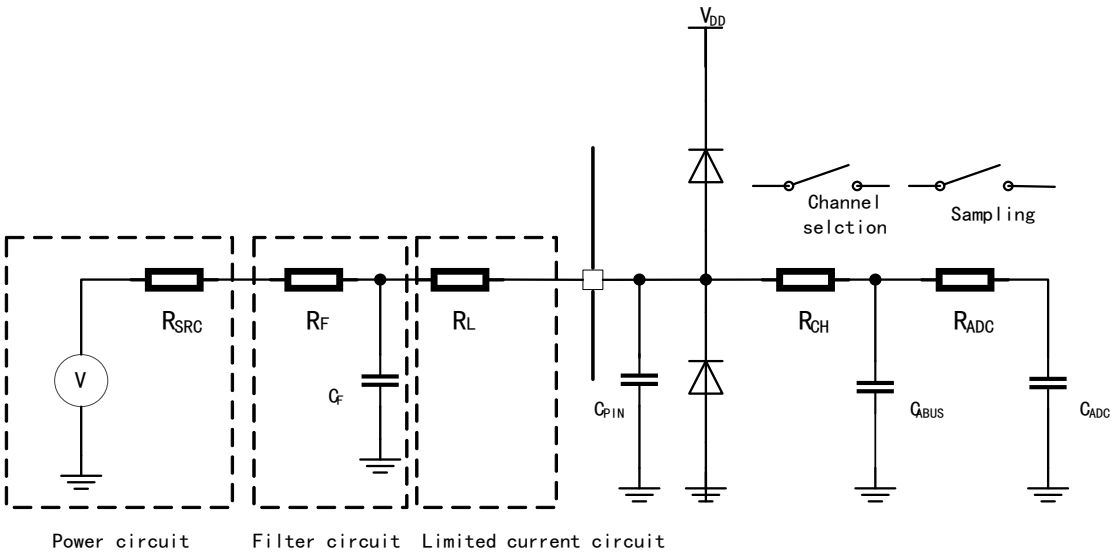


Table 39 Meanings of Symbols in ADC Input Impedance Equivalent Diagram

Symbol	Meaning
R_L	Current limiting resistance
R_{SRC}	Source impedance
R_F	Filter resistance
R_{CH}	Channel impedance
R_{ADC}	Sampling impedance
C_{ADC}	Sampling capacitance
C_{ABUS}	Analog bus capacitance
C_{PIN}	Pin capacitance
C_F	Filter capacitance

7.7.1.2 Electrical characteristics of 12-bit ADC

Notes:

(1) When two ADC are operated in parallel or simultaneous, no matter whether sampling is conducted through the same channel of two ADC or through different channels of each ADC, it may lead to reduction of ADC performance. In order to reduce the impact of synchronous conversion, it is necessary to stagger the conversions of two ADC, especially in the sampling phase.

(2) Since the ADC reference pin and power pin share the pin package, ADC simulation performance characteristics may be affected by external PCB layout. So it is necessary to pay attention to PCB wiring.

(3) All accuracy assumes that the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD} , and the calibration frequency is set to be less than or equal to half of the maximum designated ADC clock frequency.

Table 40 12-bit ADC Characteristics (V_{DD}=2.7V-4V) (V_{DDA}=V_{REFH}, V_{SS}= V_{REFL})

Symbol	Parameter	Condition	Minimum value	Typical value(1)	Maximum value	Unit
V_{DDA}	Supply voltage	-	2.7	-	4	V
I_{DDA_ADC}	Supply current of each ADC (2)	-	-	0.6	-	mA
t_S	Sampling time	-	275	-	Please refer to the *User Manual*	ns
E_T(3)	Composite error(5-9)	-	-	±4	±8	LSB(4)
E_D	Differential linear error(5-9)	-	-	±2	-	
E_L	Integral linear error(5-9)	-	-	±3	-	

Notes:

(1) Unless otherwise specified, the parameter conditions of typical values are T_A=25℃, V_{DDA}=3V, f_{ADC}=40MHz, R_{AS}=20Ω and C_{AS}=10nF.

(2) The ADC conversion rate affects the ADC supply current.

(3) Represents composite error, including offset and full-scale error.

(4) 1 LSB= (V_{REFH} - V_{REFL}) /2^N

(5) The parameter is the average value during running only in an independent mode. The performance may decrease according to the usage of the equipment. For the average value of ADC, please refer to the User Manual to determine the optimal setting of ADC_CSTS3[HAVGCFG].

(6) In the ADC signals near V_{DD}/V_{SS}, XTAL/EXTAL or high-frequency switch pins, the performance of ADC may decrease.

(7) These values can ensure the performance of the ADC on multiple ADC input channel pins. When ADC is used to monitor internal analog parameters, it is assumed that the performance decreases.

(8) All parameters in the table are parameters of the ADC clock source provided by the system clock.

(9) In high and low temperature environments, it is recommended that the ADC clock be 16MHz to ensure the accuracy of the results.

Table 41 12-bit ADC Characteristics (V_{DD}=4V-5.5V) (V_{DDA} =V_{REFH}, VSS =V_{REFL})

Symbol	Parameter	Condition	Minimum value	Typical value(1)	Maximum value	Unit
V_{DDA}	Supply voltage	-	4	-	5.5	V
I_{DDA_ADC}	Supply current of each ADC(2)	-	-	1	-	mA
t_S	Sampling time	-	275	-	Please refer to the *User Manual*	ns
E_T(3)	Composite error(5-9)	-	-	±4	±8	LSB(4)
E_D	Differential non-linearity(5-9)	-	-	±1.5	-	
E_L	Integral non-linearity(5-9)	-	-	±2	-	

Notes:

(1) Unless otherwise specified, the parameter conditions of typical values are T_A=25℃, V_{DDA}=5V, f_{ADC}=40MHz, R_{AS}=20Ω and C_{AS}=10nF.

(2) The ADC conversion rate affects the ADC supply current.

(3) Represents static error, including offset and full-scale error.

(4) 1 LSB= (V_{REFH} - V_{REFL}) /2^N

(5) The parameter is the average value during running only in an independent mode. The performance may decrease according to the usage of the equipment. For the average value of ADC, please refer to the User Manual to determine the optimal setting of ADC_CSTS3[HAVGCFG].

(6) In the ADC signals near V_{DD}/V_{SS}, XTAL/EXTAL or high-frequency switch pins, the performance of ADC may decrease.

(7) These values can ensure the performance of the ADC on multiple ADC input channel pins. When ADC is used to monitor internal analog parameters, it is assumed that the performance decreases.

(8) All parameters in the table are parameters of the ADC clock source provided by the system clock.

Notes:

(1) The use of triple bonding in packages such as LQFP100 and LQFP64 can lead to a decrease in ADC performance.

7.7.2 Comparator with internal 8-bit DAC

Table 42 Electrical Characteristics of Comparator with internal 8-bit DAC

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
I_{DDH}	Supply current (1)	High-speed mode	-40℃ - 125℃	-	230	300	μA
I_{DDL}		Low-speed mode	-40℃ - 125℃	-	6	13	
V_{IN}	DAC input voltage(Analog input voltage) (1)	-		0	0-V_{DDA}	V_{DDA}	V
V_{OSH}	Input offset voltage	High-speed mode	-40℃ - 125℃	-25	±1	25	mV
V_{OSL}	Input offset voltage	Low-speed mode	-40℃ - 125℃	-40	±4	40	
t_{PDH_100}	Propagation delay(2)	High-speed mode	-40℃ - 125℃	-	35	300	ns
t_{PDL_100}		Low-speed mode	-40℃ - 125℃	-	0.5	3	μs
t_{PDH_30}	Propagation delay(3)	High-speed mode	-40℃ - 125℃	-	70	500	ns
t_{PDL_30}		Low-speed mode	-40℃ - 125℃	-	1	5	μs
t_{IDH}	Initialization delay(4)	High-speed mode	-40℃ - 125℃	-	1.5	3	
t_{IDL}		Low-speed mode	-40℃ - 125℃	-	10	30	
V_{hyst0}	Analog comparator hysteresis	hyst0	-40℃ - 125℃	-	0	-	mV
V_{hyst1}		hyst1 High-speed mode	-40℃ - 125℃	-	19	66	

Symbol	Parameter	Condition		Minimum value	Typical value	Maximum value	Unit
		hyst1 Low-speed mode	-40℃ - 125℃	-	15	40	
V_{hyst2}		hyst2 High-speed mode	-40℃ - 125℃	-	34	133	
		hyst2 Low-speed mode	-40℃ - 125℃	-	23	80	
V_{hyst3}		hyst3 High-speed mode	-40℃ - 125℃	-	46	200	
		hyst3 Low-speed mode	-40℃ - 125℃	-	32	120	
I_{DAC8}	8-bit DAC current adder (enabled)	3.3V reference voltage		-	6	9	μA
		5V reference voltage		-	10	16	
E_D	Differential linear error	-		-0.5	-	0.5	LSB(6)
E_L	Integral linear error(5)	-		-0.75	-	0.75	
t_{IS}	Initialization and switching stability time	-		-	-	30	μs

Notes:

(1) Voltage input difference of $I_{DDH/DDL}$ is >200mV

(2) Apply ±(100mV + $V_{hyst0/1/2/3}$ + maximum $V_{OSH/OSL}$) around the switching point.

(3) Apply ±(30mV + 2 * $V_{hyst0/1/2/3}$ + maximum $V_{OSH/OSL}$) around the switching point.

(4) Apply ±(100mV + $V_{hyst0/1/2/3}$).

(5) Calculate through linear regression least square method.

(6) 1LSB=reference voltage/256

Note: If the input signal of the comparator is close to V_{DD}/V_{SS} or XTAL/EXTAL or switch pins, cross coupling may occur, which can be solved by setting hysteresis to obtain the comparator performance. Besides, when performing noise filtering on the input signals, an external capacitor (1nF) shall be used. And the source driver shall not be weak (it is recommended that the signal pull up/pull down be less than 50K).

The curve below shows Level-3 hysteresis, Level-2 hysteresis, Level-1 hysteresis, and Level-0 hysteresis from top to bottom.

Figure 15 Typical hysteresis vs. Vin level(V_{DDA}=3.3V,PMSEL=0)

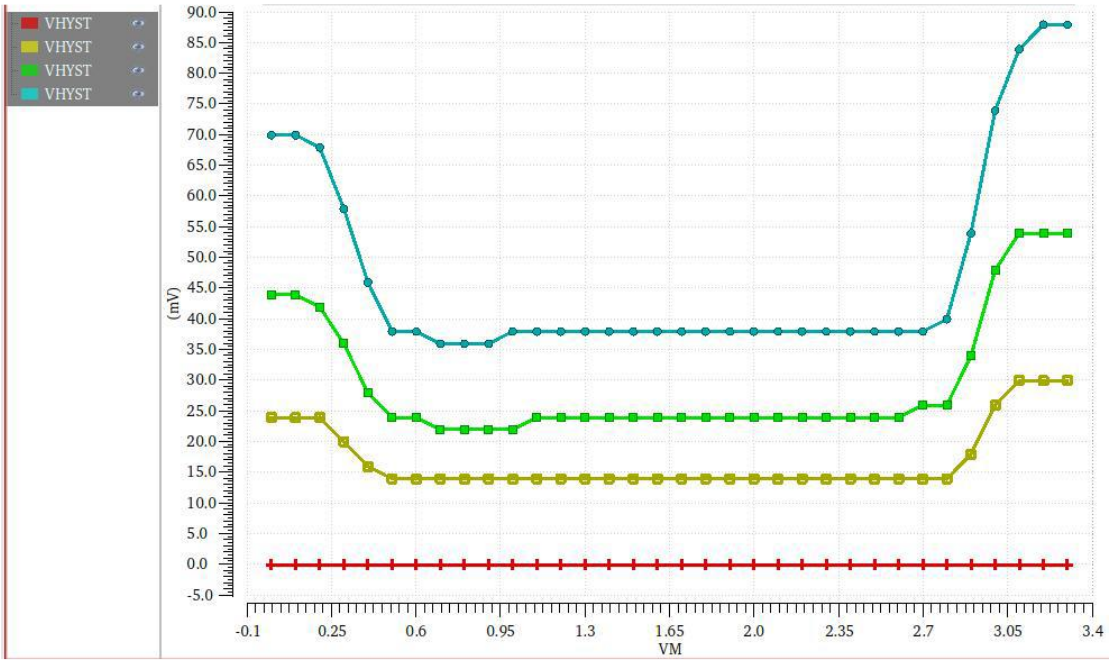


Figure 16 Typical hysteresis vs. Vin level(V_{DDA}=3.3V,PMSEL=1)

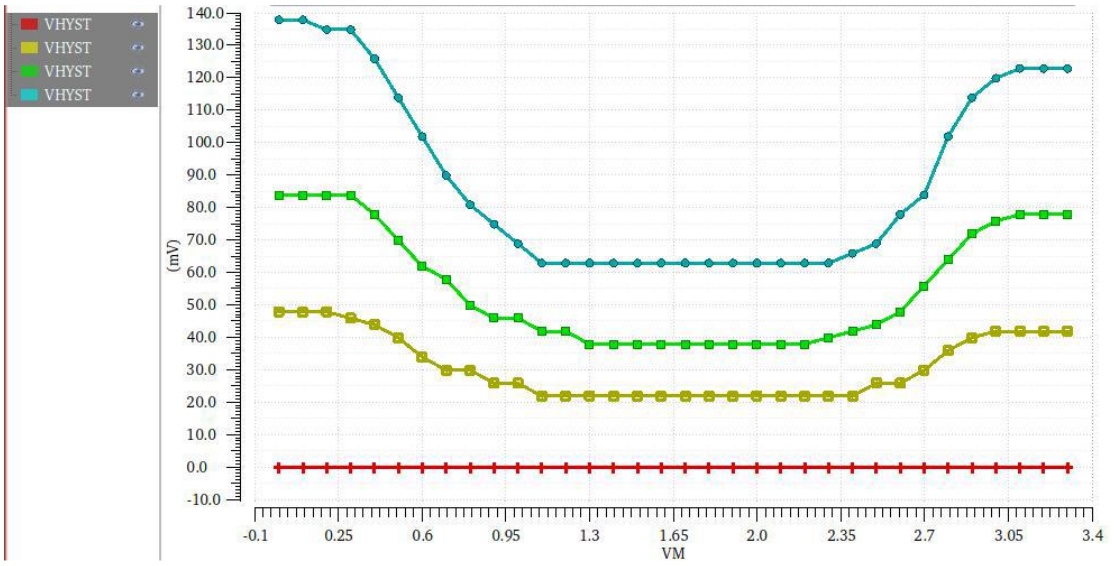


Figure 17 Typical hysteresis vs. Vin level(V_{DDA}=5V,PMSEL=0)

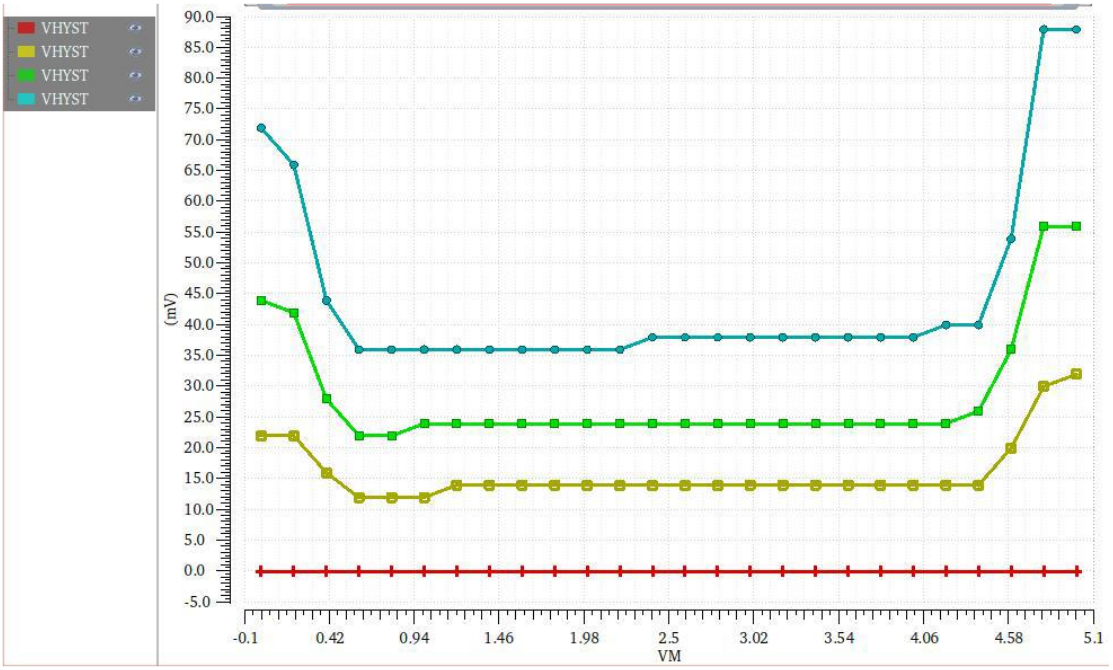
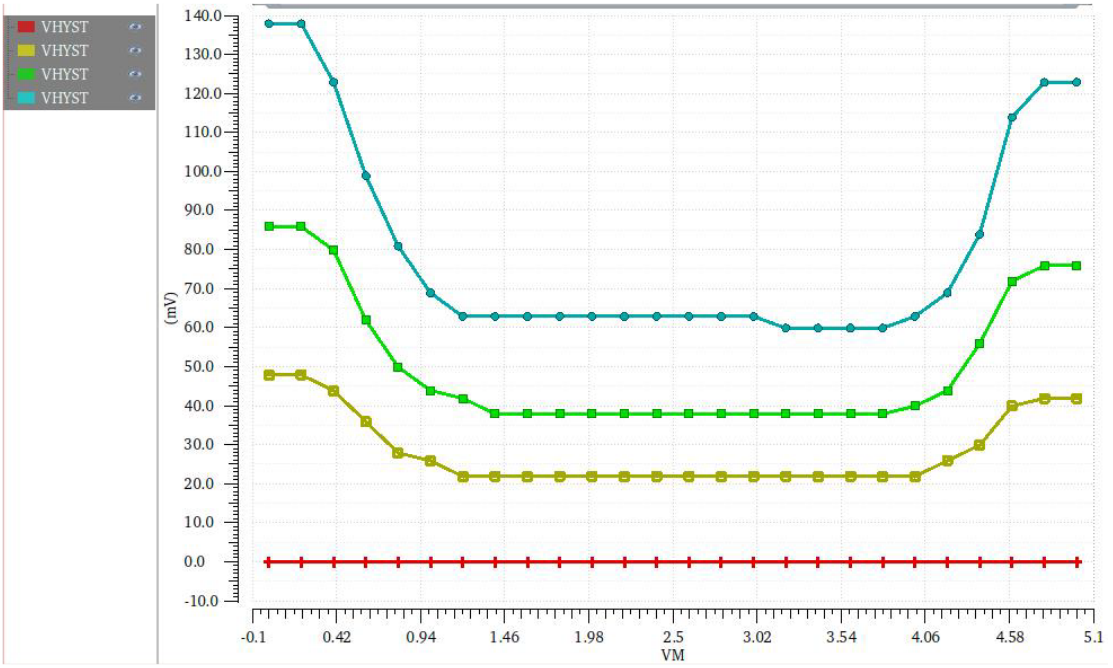


Figure 18 Typical hysteresis vs. Vin level(V_{DDA}=5V,PMSEL=1)



7.8 Debugging module

7.8.1 SWD electrical specifications

7.8.1.1 Electrical specifications for SWD run mode

Table 43 Electrical Specification for SWD Run Mode

Symbol	Parameter	Condition	Operation Modes						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_{SWCIK}	SWD clock operating frequency	-	-	-	25	-	-	25	MHz
t_{SWCIK}	SWD clock cycle	-	$1/f_{SWDCLK}$	-	-	$1/f_{SWDCLK}$	-	-	ns
$t_{r(SWCIK)}$ $t_{f(SWCIK)}$	SWD clock rise and fall time	-	-	-	5	-	-	5	
$t_{cpw(SWCIK)}$	SWCLK clock pulse width	-	$t_{SWDCLK}/2-5$	-	$t_{SWDCLK}/2+5$	$t_{SWDCLK}/2-5$	-	$t_{SWDCLK}/2+5$	
$t_{su(SWCIK)}$	Before the SWD clock rises, SWDIO input data setup time	-	4	-	-	4	-	-	
$t_{h(SWDIO)}$	After the SWD clock rises, SWDIO input data hold time	-	3	-	-	3	-	-	
$t_{v(SWD)}$	SWD clock high to SWDIO data valid	-	-	-	38	-	-	29	
$t_{iv(SWD)}$	SWD clock high to SWDIO data invalid	-	0	-	-	0	-	-	

Symbol	Parameter	Condition	Operation Modes						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
$t_{h-Z(SWD)}$	SWD clock high to SWDIO high resistance	-	-	-	38	-	-	34	

7.8.1.2 Electrical specifications for SWD high-speed run mode

Table 44 Electrical Specification for SWD High-speed Run Mode

Symbol	Parameter	Condition	High-speed run mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_{SWCIK}	SWD clock operating frequency	-	-	-	25	-	-	25	MHz
t_{SWCIK}	SWD clock cycle	-	$1/f_{SWDCLK}$	-	-	$1/f_{SWDCLK}$	-	-	ns
$t_{r(SWCIK)}$ $t_{f(SWCIK)}$	SWD clock rise and fall time	-	-	-	6	-	-	6	
$t_{cpw(SWCIK)}$	SWCLK clock pulse width	-	$t_{SWDCLK}/2-5$	-	$t_{SWDCLK}/2+5$	$t_{SWDCLK}/2-5$	-	$t_{SWDCLK}/2+5$	
$t_{su(SWCIK)}$	Before the SWD clock rises, SWDIO input data setup time	-	4	-	-	4	-	-	
$t_{h(SWDIO)}$	After the SWD clock rises,SWDIO input data hold time	-	3	-	-	3	-	-	
$t_{v(SWD)}$	SWD clock high to SWDIO data valid	-	-	-	38	-	-	29	

Symbol	Parameter	Condition	High-speed run mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
$t_{iv(SWD)}$	SWD clock high to SWDIO data invalid	-	0	-	-	0	-	-	
$t_{h-Z(SWD)}$	SWD clock high to SWDIO high resistance	-	-	-	38	-	-	34	

7.8.1.3 Electrical characteristics of SWD VLPR mode

Table 45 Electrical Specification for SWD VLPR Mode

Symbol	Parameter	Condition	VLPR mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_{SWCIK}	SWD clock operating frequency	-	-	-	10	-	-	10	MHz
t_{SWCIK}	SWD clock cycle	-	$1/f_{SWDCLK}$	-	-	$1/f_{SWDCLK}$	-	-	ns
$t_{r(SWCIK)}$ $t_{f(SWCIK)}$	SWD clock rise and fall time	-	-	-	4	-	-	4	
$t_{cpw(SWCIK)}$	SWCLK clock pulse width	-	$t_{SWDCLK}/2-5$	-	$t_{SWDCLK}/2+5$	$t_{SWDCLK}/2-5$	-	$t_{SWDCLK}/2+5$	
$t_{su(SWCIK)}$	Before the SWD clock rises, SWDIO input data setup time	-	16	-	-	16	-	-	
$t_{h(SWDIO)}$	After the SWD clock rises,SWDIO input data hold time	-	10	-	-	10	-	-	

Symbol	Parameter	Condition	VLPR mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
$t_{v(SWD)}$	SWD clock high to SWDIO data valid	-	-	-	77	-	-	70	
$t_{iv(SWD)}$	SWD clock high to SWDIO data invalid	-	0	-	-	0	-	-	
$t_{h-Z(SWD)}$	SWD clock high to SWDIO high resistance	-	-	-	77	-	-	70	

Figure 19 SWD Clock Input Time

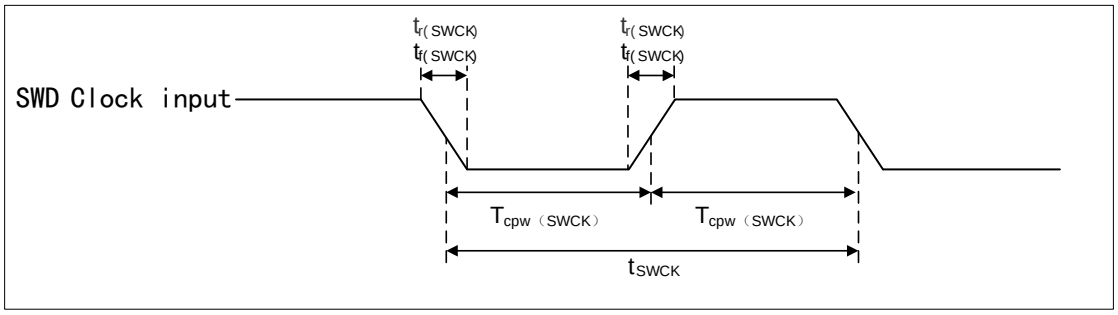
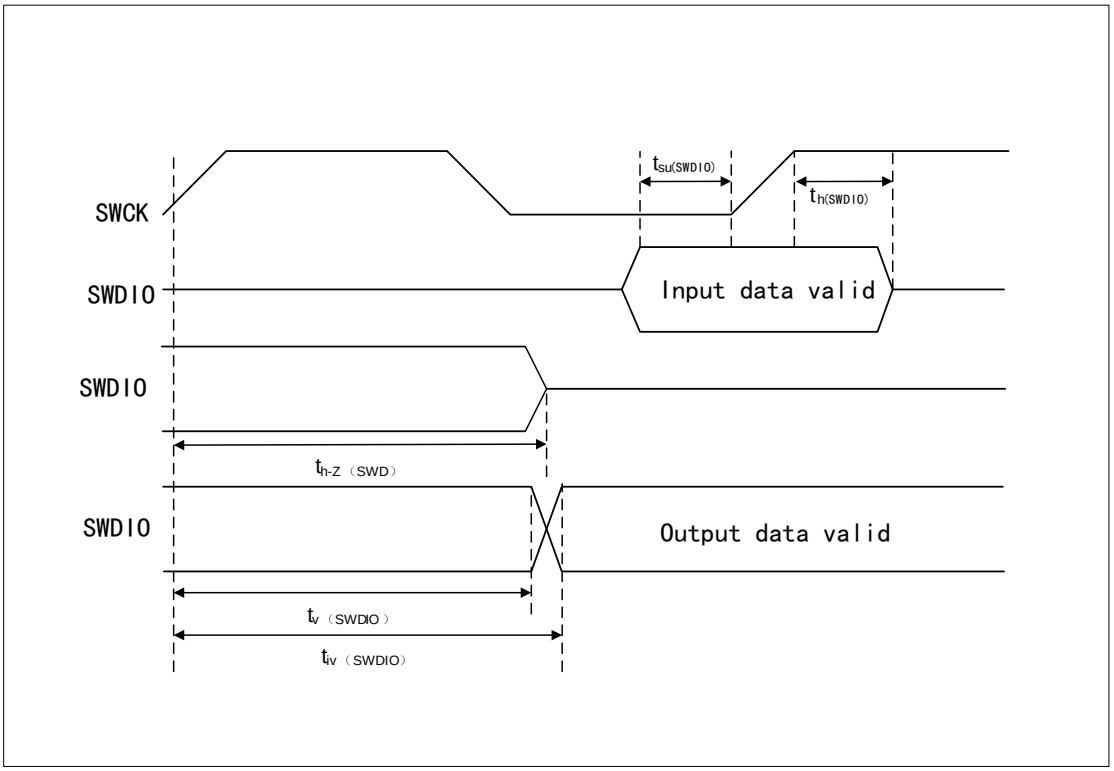


Figure 20 SWD Input/Output Data Time



7.8.2 Electrical characteristics of JTAG

7.8.2.1 Electrical characteristics of JTAG run mode

Table 46 Electrical Characteristics of JTAG Run Mode

Symbol	Parameter	Condition	Operation Modes						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_{TCLK}	TCLK operating frequency	Boundary scan	-	-	20	-	-	20	MHz
		JTAG	-	-	20	-	-	20	ns
$t_{cpw(TCLK)}$	TCLK clock pulse width	Boundary scan / JTAG	t_{TCLK}/2-5	-	t_{TCLK}/2+5	t_{TCLK}/2-5	-	t_{TCLK}/2+5	
t_{TCLK}	TCLK cycle	-	$1/f_{TCLK}$	-	-	$1/f_{TCLK}$	-	-	
$t_{r(TCLK)}$ $t_{f(TCLK)}$	TCLK rise and fall time	-	-	-	3	-	-	3	
$t_{v(BSO)}$	TCLK low to boundary scan output data valid	-	-	-	32	-	-	28	
$t_{iv(BSO)}$	TCLK low to boundary scan output data invalid	-	0	-	-	0	-	-	
$t_{v(TDO)}$	TCLK low to TDO data valid	-	-	-	32	-	-	28	
$t_{iv(TDO)}$	TCLK low to TDO data invalid	-	0	-	-	0	-	-	

Symbol	Parameter	Condition	Operation Modes						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
$t_{su(BSI)}$	Boundary scan input data setup time	TCLK rises	5	-	-	5	-	-	
$t_{h(BSI)}$	Boundary scan input data hold time	After TCLK rises	5	-	-	5	-	-	
$t_{h-Z(BS)}$	Output high resistance	TCLK is lower than boundary scan	-	-	32	-	-	28	
$t_{h-Z(TDO)}$	Output high resistance	When TCLK is lower than TDO	-	-	32	-	-	28	
$t_{su(TTI)}$	TMS and TDI input data setup time	TCLK rises	3	-	-	3	-	-	
$t_{h(TTI)}$	TMS and TDI input data hold time	After TCLK rises	2	-	-	2	-	-	

7.8.2.2 Electrical characteristics of JTAG high-speed run mode

Table 47 Electrical Characteristics of JTAG High-speed Run Mode

Symbol	Parameter	Condition	High-speed run mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_{TCLK}	TCLK operating frequency	Boundary scan	-	-	20	-	-	20	MHz
		JTAG	-	-	20	-	-	20	ns
$t_{cpw(TCLK)}$	TCLK clock	Boundary scan	t_{TCLK}/2-5	-	t_{TCLK}/2+5	t_{TCLK}/2-5	-	t_{TCLK}/2+5	

Symbol	Parameter	Condition	High-speed run mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
	pulse width	JTAG							
t_{TCLK}	TCLK cycle	-	$1/f_{TCLK}$	-	-	$1/f_{TCLK}$	-	-	
$t_{r(TCLK)}$ $t_{f(TCLK)}$	TCLK rise and fall time	-	-	-	3	-	-	3	
$t_{v(BSO)}$	TCLK low to boundary scan output data valid	-	-	-	32	-	-	28	
$t_{iv(BSO)}$	TCLK low to boundary scan output data invalid	-	0	-	-	0	-	-	
$t_{v(TDO)}$	TCLK low to TDO data valid	-	-	-	32	-	-	28	
$t_{iv(TDO)}$	TCLK low to TDO data invalid	-	0	-	-	0	-	-	
$t_{su(BSI)}$	Before TCLK rises, boundary scan input data setup time	-	5	-	-	5	-	-	

Symbol	Parameter	Condition	High-speed run mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
$t_{h(BSI)}$	After TCLK rises, boundary scan input data hold time	-	5	-	-	5	-	-	
$t_{h-Z(BS)}$	TCLK falling edge to boundary scan output high resistance	-	-	-	32	-	-	28	
$t_{h-Z(TDO)}$	TCLK falling edge to TDO high resistance	-	-	-	32	-	-	28	
$t_{su(TTI)}$	Before TCLK rises,TMS and TDI input data setup time	-	3	-	-	3	-	-	
$t_{h(TTI)}$	After TCLK rises,TMS and TDI input data hold time	-	2	-	-	2	-	-	

7.8.2.3 Electrical characteristics of TAG VLPR mode

Table 48 Electrical Characteristics of JTAG VLPR Mode

Symbol	Parameter	Condition	VLPR mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
f_{TCLK}	TCLK operating frequency	Boundary scan	-	-	10	-	-	10	MHz
		JTAG	-	-	10	-	-	10	ns
$t_{cpw(TCLK)}$	TCLK clock pulse width	Boundary scan / JTAG	t_{TCLK}/2-5	-	t_{TCLK}/2+5	t_{TCLK}/2-5	-	t_{TCLK}/2-5	
t_{TCLK}	TCLK cycle	-	$1/f_{TCLK}$	-	-	$1/f_{TCLK}$	-	$1/f_{TCLK}$	
$t_{r(TCLK)}$ $t_{f(TCLK)}$	TCLK rise and fall time	-	-	-	3	-	-	3	
$t_{v(BSO)}$	TCLK low to boundary scan output data valid	-	-	-	80	-	-	80	
$t_{iv(BSO)}$	TCLK low to boundary scan output data invalid	-	0	-	-	0	-	-	
$t_{v(TDO)}$	TCLK low to TDO data valid	-	-	-	80	-	-	80	

Symbol	Parameter	Condition	VLPR mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
$t_{iv(TDO)}$	TCLK low to TDO data invalid	-	0	-	-	0	-	-	
$t_{su(BSI)}$	Before TCLK rises, boundary scan input data setup time		15	-	-	15	-	-	
$t_{h(BSI)}$	After TCLK rises, boundary scan input data hold time		8	-	-	8	-	-	
$t_{h-Z(BS)}$	TCLK falling edge to boundary scan output high resistance		-	-	80	-	-	80	
$t_{h-Z(TDO)}$	TCLK falling edge to TDO high resistance		-	-	80	-	-	80	

Symbol	Parameter	Condition	VLPR mode						Unit
			3.3V IO			5V IO			
			Minimum value	Typical value	Maximum value	Minimum value	Typical value	Maximum value	
$t_{su(TTI)}$	Before TCLK rises, TMS and TDI input data setup time		15	-	-	15	-	-	
$t_{h(TTI)}$	After TCLK rises, TMS and TDI input data hold time		8	-	-	8	-	-	

Figure 21 TCLK Input Timing

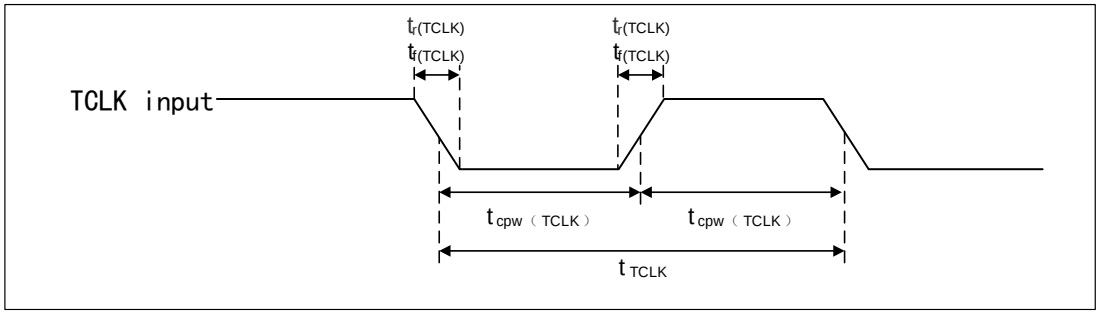


Figure 22 JTAG Boundary Scan Timing

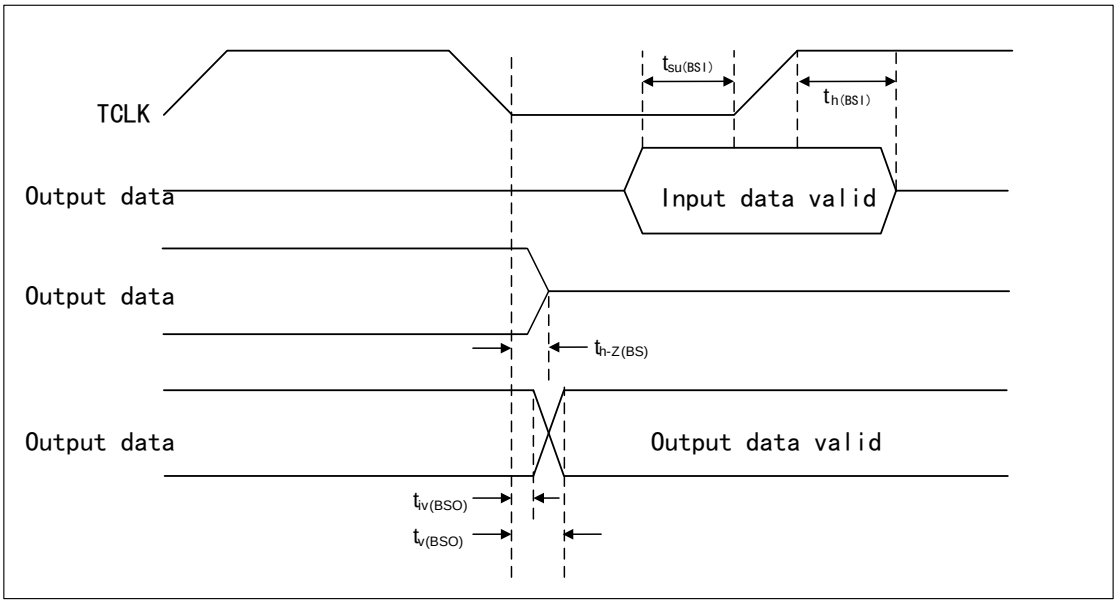
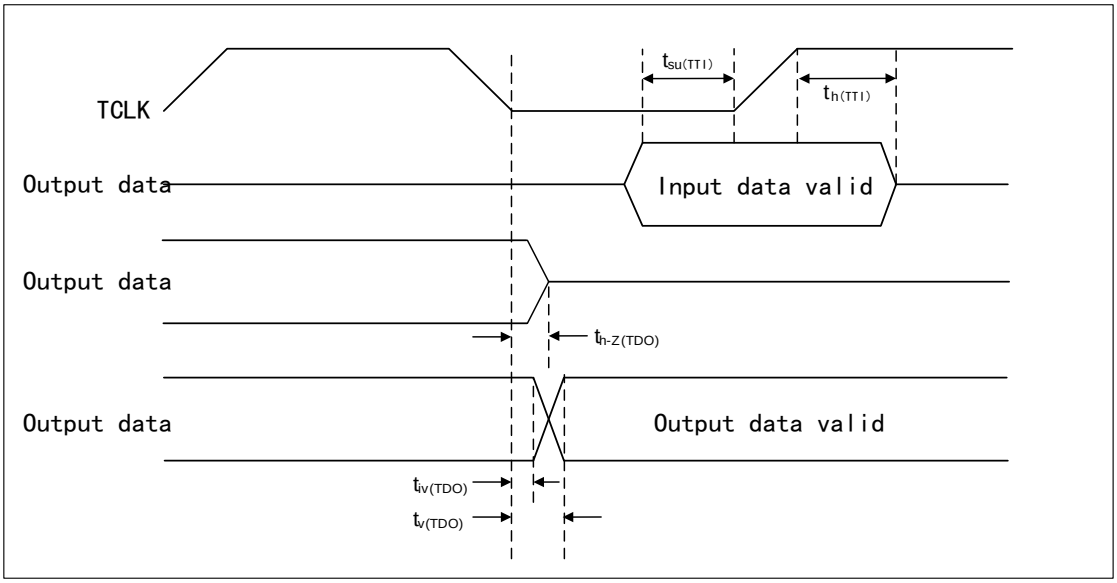


Figure 23 TDO Timing



7.9 Temperature characteristics

7.9.1 General precautions for specifications at maximum junction temperature

Calculation of chip junction temperature T_J can be obtained from the following equation:

$$T_J = (R_{\theta JA} \times P_D) + T_A$$

Where: $R_{\theta JA}$ represents the thermal resistance of the joint to the environment (℃/W), P_D represents the power dissipation of the package (W), and T_A represents the ambient temperature of the packaging (℃).

The thermal resistance connected to the environment is an industry standard value, and can be used to estimate the temperature characteristics quickly and conveniently. Usually it is determined by two values: the determined of the single-layer boards and the value measured on the double-layer boards. Which value is closer to the application depends on the power consumed by other components on the board. The values on the single-layer boards are applicable to tightly encapsulated printed circuit boards; if the power consumption of the board is low and the components are well separated, the value obtained on the board with an internal plane is more suitable.

When using a radiator, the thermal resistance in the following equation is expressed as the sum of the thermal resistance connected to the shell and the ambient thermal resistance:

$$R_{\theta JA} = R_{\theta CA} + R_{\theta JC}$$

Where: $R_{\theta JA}$ represents the thermal resistance (℃/W) of the joint to the environment, $R_{\theta CA}$ represents ambient thermal resistance (℃/W), and $R_{\theta JC}$ represents the thermal resistance (℃/W) of the joint to the shell.

The value of $R_{\theta JC}$ is related to the equipment and is not controlled by users. Users can change the instance to the ambient thermal resistance $R_{\theta CA}$ by controlling the thermal environment. For example, users can change the heat dissipation of the printed circuit board around the equipment, the airflow around the equipment, interface materials, wiring on the printed circuit board, or dimensions of the radiator.

When the radiator is not used, the thermal characterization parameters (ψ_{JT}) can be used to determine the junction temperature of the device in the application, and the following equation can be used to measure the center temperature at the top of the package shell:

$$T_J = T_T + (\psi_{JT} \times P_D)$$

Where: T_T represents the temperature of the thermocouple at the top of the package (℃), ψ_{JT} represents the thermal characterization parameter (℃/W), and P_D represents the power dissipation of the package (W).

According to the JESD51-2 standard, the temperature characteristic parameters are measured with a No. 40 T-type thermocouple connected to the center of the top of the package with epoxy resin.

Note:

(1) The thermocouple wire shall be laid flat on the package shell to avoid measurement errors caused by the cooling effect of the thermocouple wires.

(2) Ensure that the thermocouple junction is located on the package. Place a small amount of epoxy resin on the thermocouple junction and place it on the approximately 1mm wire extending from the junction.

7.9.2 Temperature characteristics

Table 49 Temperature Characteristics

Symbol	Parameter	Condition	Package		Unit
			LQFP64	LQFP100	
$R_{\theta JA}$(1)	Thermal resistance, joint to the environment (natural convection)	Single-layer board (1s)	61	52	℃/W
		Double-layer board (1s1p)	45	42	℃/W
		Four-layer board (2s2p)	43	40	℃/W
$R_{\theta JMA}$(1)	Thermal resistance, jointto the environment (forced convection, 200 feet/min)	Single-layer board (1s)	49	42	℃/W
		Double-layer board (1s1p)	38	35	℃/W
		Four-layer board (2s2p)	36	34	℃/W
$R_{\theta JC}$(2)	Thermal resistance, joint to the shell	-	12	12	℃/W
$R_{\theta JB}$(3)	Thermal resistance, joint to the board	-	25	25	℃/W
ψ_{JT}(4)	Thermal resistance, joint to the top of the package	Natural convection	2	2	℃/W

Notes:

(1) The size of tube core, thermal resistance of package, thermal resistance of board, ambient temperature, installation position (board) temperature, air flow rate, power consumption on the chip, and power consumption of other components on the board all affect the junction temperature, and the junction temperature is a function of these parameters.

(2) Indicates the thermal resistance between the mold and the surface of the shell, measured through the cold plate method.

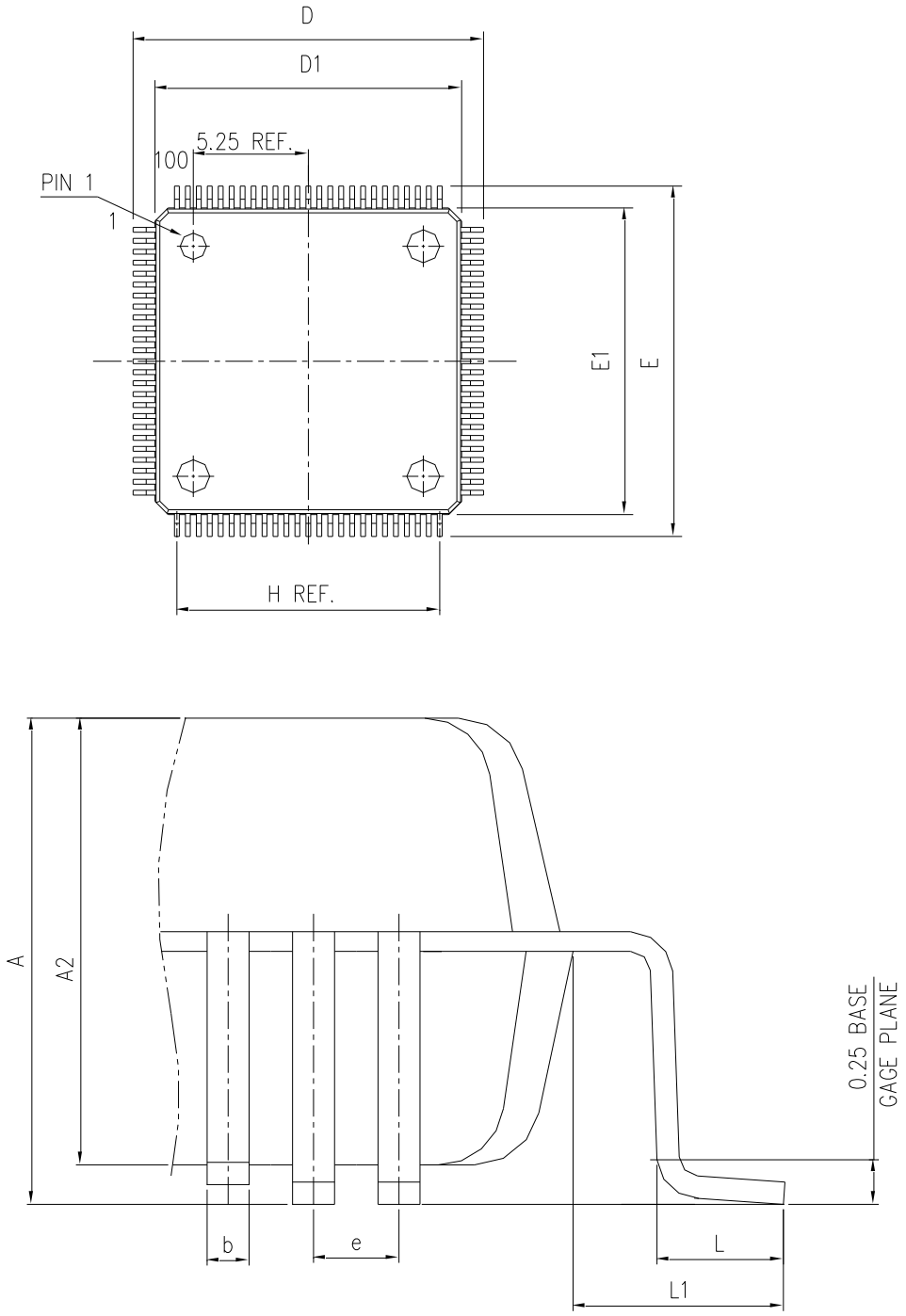
(3) Indicates the thermal resistance between the chip and the printed circuit board. The temperature of the board is measured on the top surface of the board near the package.

(4) Thermal characterization parameter, indicating the temperature difference between the junction temperature and the top of the package. When Greek alphabet is not available, this parameter will be expressed as Psi JT.

8 Package Information

8.1 LQFP100 package information

Figure 24 LQFP100 Package Diagram



(1) The figure is not drawn to scale.

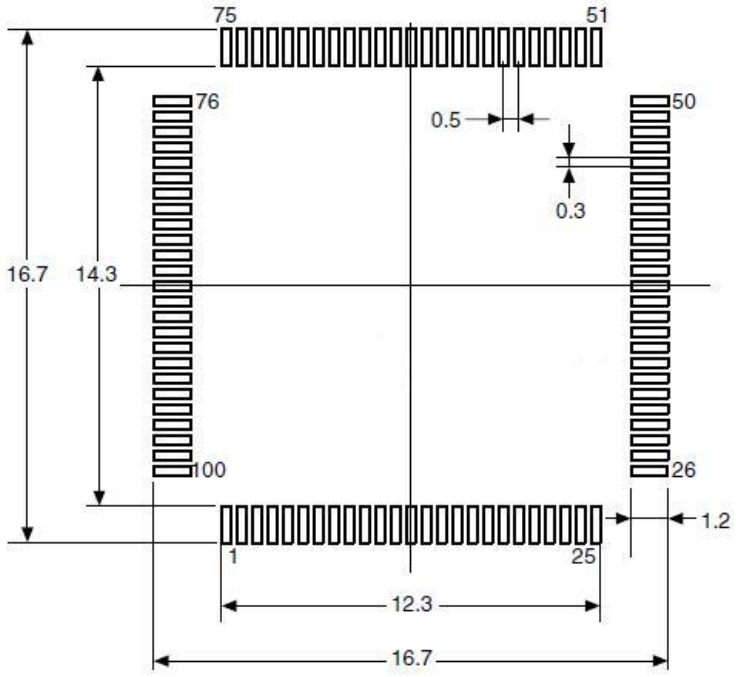
(2) All pins should be soldered to the PCB.

Table 50 LQFP100 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENDIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H (REF)	(12.00)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

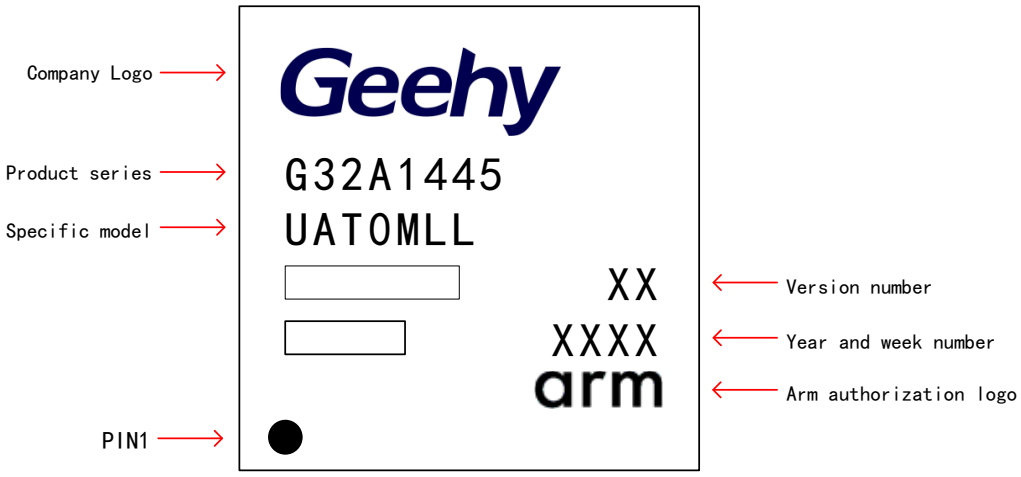
Note: Dimensions are marked in millimeters.

Figure 25 LQFP100 - 100 Pins, 14 x 14mm Welding Layout Recommendations



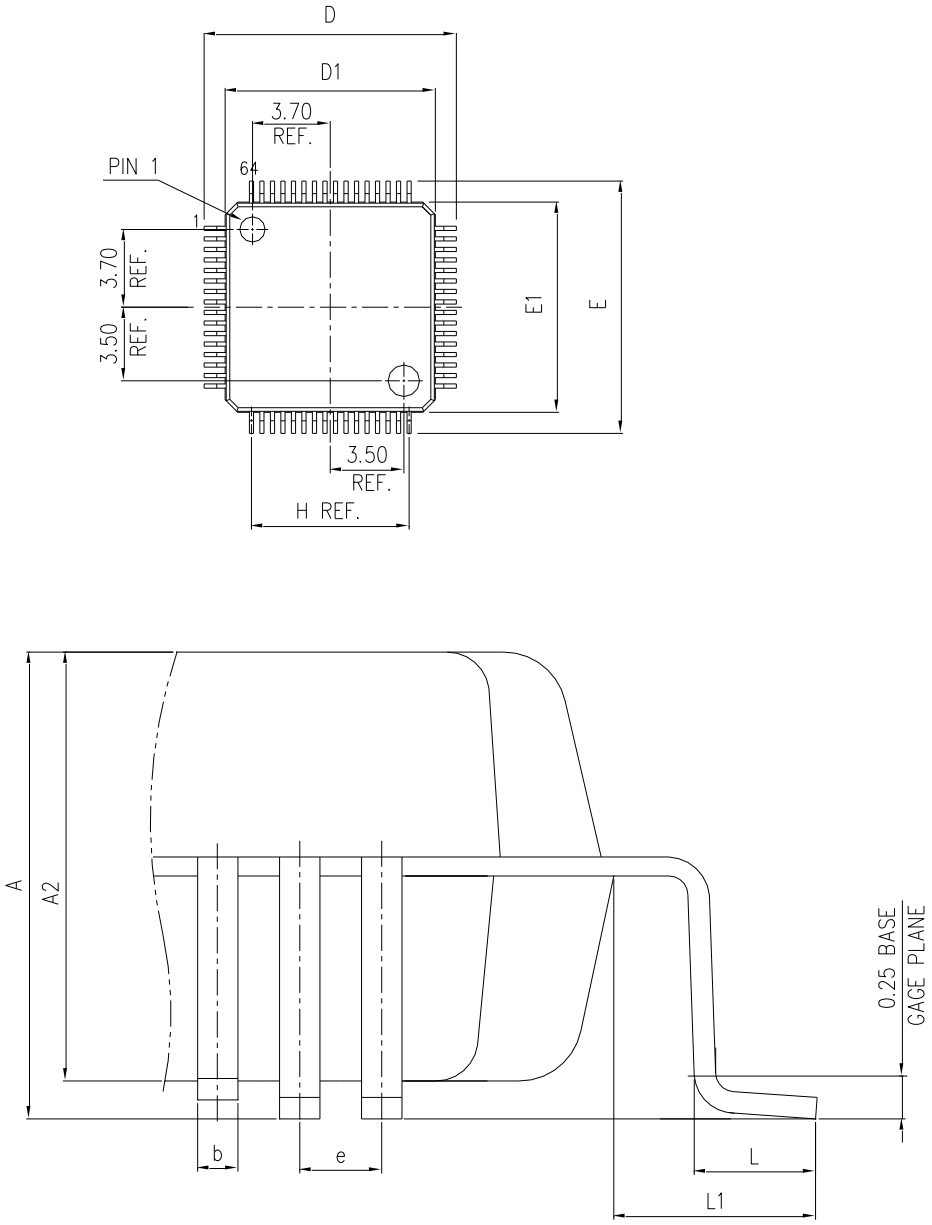
Note: Dimensions are marked in millimeters.

Figure 26 LQFP100 - 100 Pins, 14 x 14mm Diagram



8.2 LQFP64 package information

Figure 27 LQFP64 Package Diagram



(1) The figure is not drawn to scale.

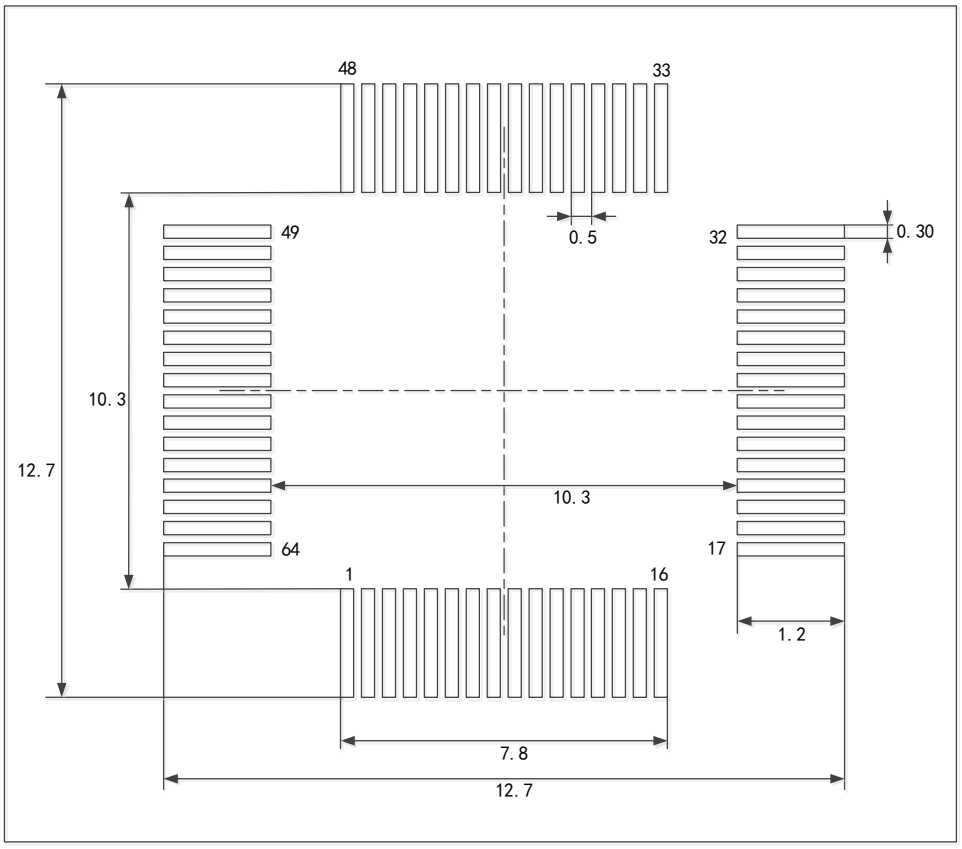
(2) All pins should be soldered to the PCB.

Table 51 LQFP64 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.600	OVERALLHEIGHT
2	A2	1.400±0.050	PKGTHICKNESS
3	D	12.000±0.200	LEADTIPTOTIP
4	D1	10.000±0.100	PKGLENGTH
5	E	12.000±0.200	LEADTIPTOTIP
6	E1	10.000±0.100	PKGWIDTH
7	L	0.600±0.150	FOOTLENGTH
8	L1	1.000REF.	LEADLENGTH
9	e	0.500BASE	LEADPITCH
10	H(REF.)	(7.500)	GUM.LEADPITCH
11	b	0.220±0.050	LEADWIDTH

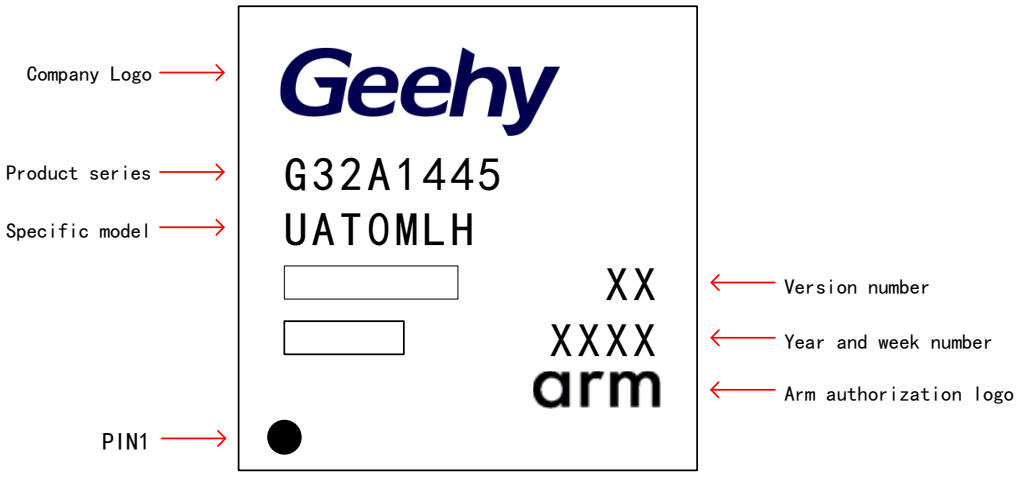
Note: Dimensions are marked in millimeters.

Figure 28 LQFP64 Welding Layout Recommendations



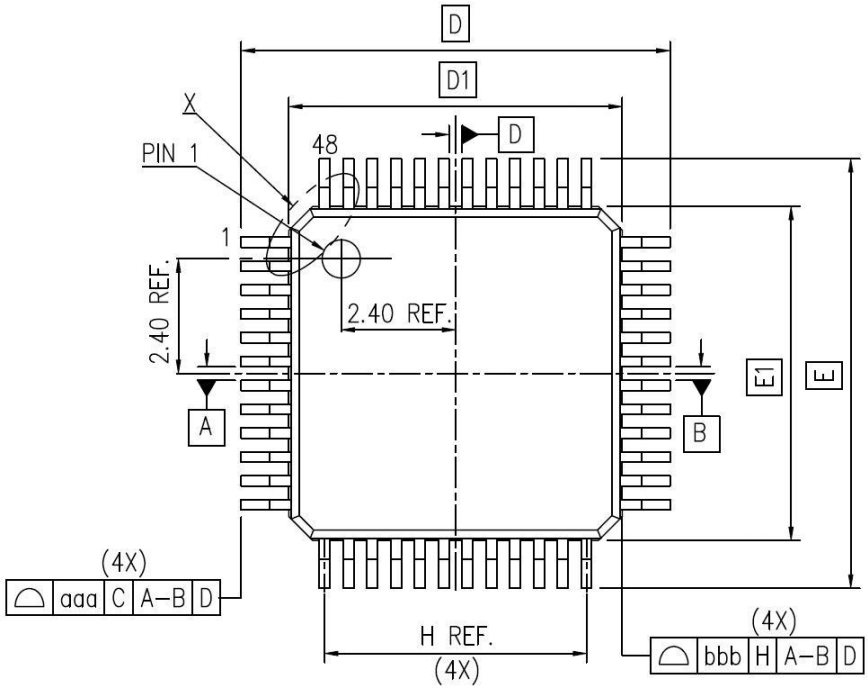
Note: Dimensions are marked in millimeters.

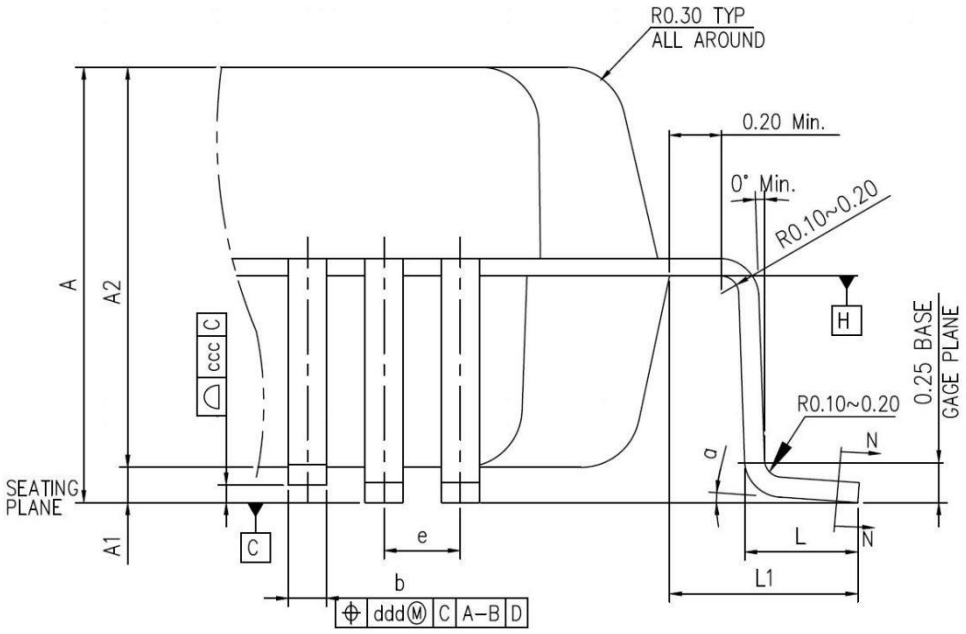
Figure 29 LQFP64 - 64 Pins, 10 x 10mm Diagram



8.3 LQFP48 package information

Figure 30 LQFP48 Package Diagram





(1) The figure is not drawn to scale.

(2) All pins should be soldered to the PCB.

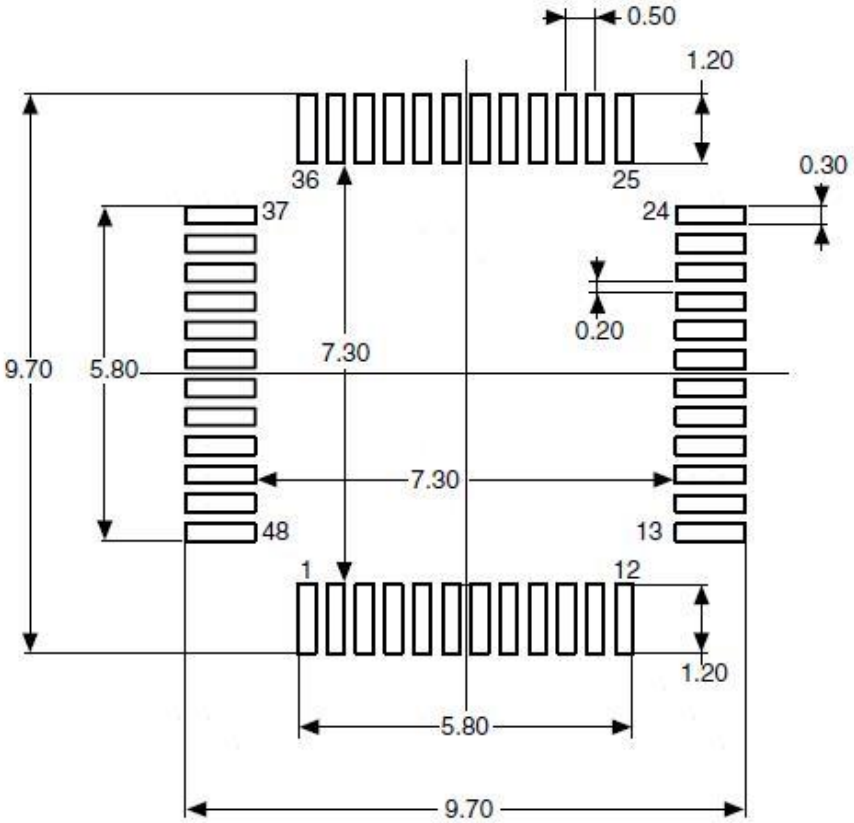
Table 52 LQFP48 Package Data

DIMENSION LIST(FOOTPRINT: 2.00)			
S/N	SYM	DIMENDIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.1±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	9.00±0.20	LEAD TIP TO TIP
5	D1	7.00±0.10	PKG LENGTH
6	E	9.00±0.20	LEAD TIP TO TIP
7	E1	7.00±0.10	PKG WDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF	LEAD LENGTH
10	T	0.15	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.02	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(5.50)	CUM. LEAD PITCH
17	aaa	0.2	PROFILE OF LEAD TIPS

DIMENSION LIST(FOOTPRINT: 2.00)			
18	bbb	0.2	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

Note: Dimensions are marked in millimeters.

Figure 31 LQFP48 Welding Layout Recommendations



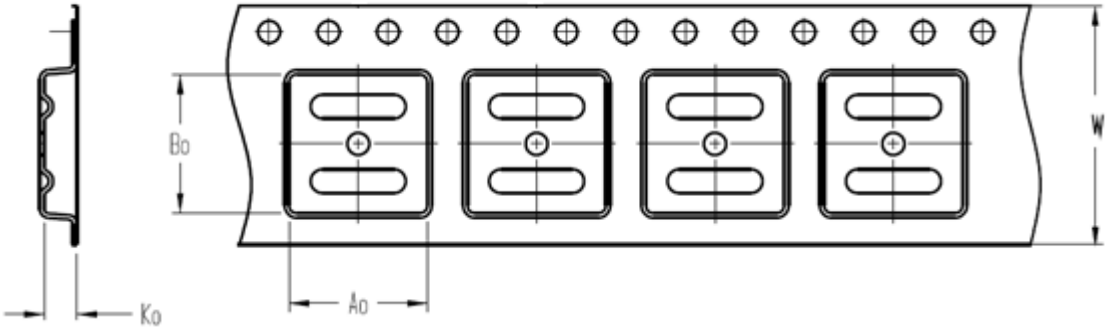
Note: Dimensions are marked in millimeters.

Figure 32 LQFP64 - 64 Pins, 7 x 7mm Diagram

9 Packaging Information

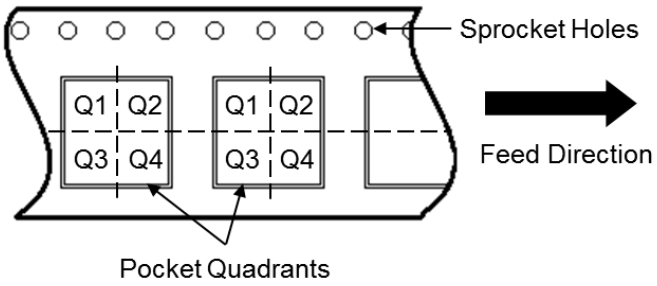
9.1 Reel Packaging

Figure 33 Reel Packaging Specification Drawing

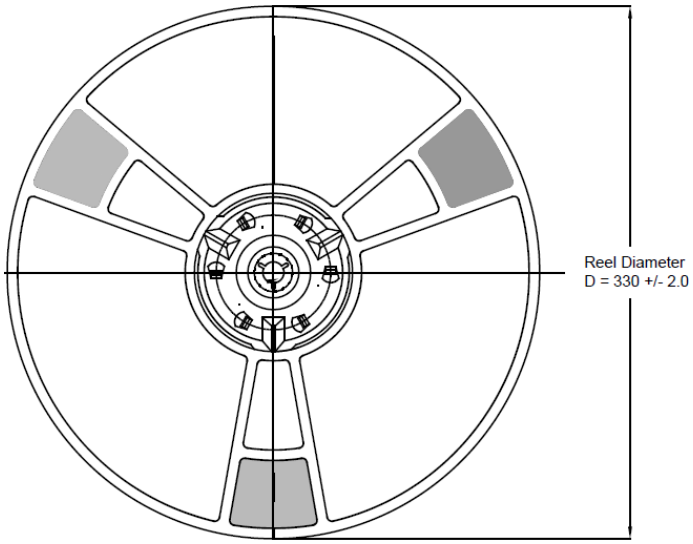


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



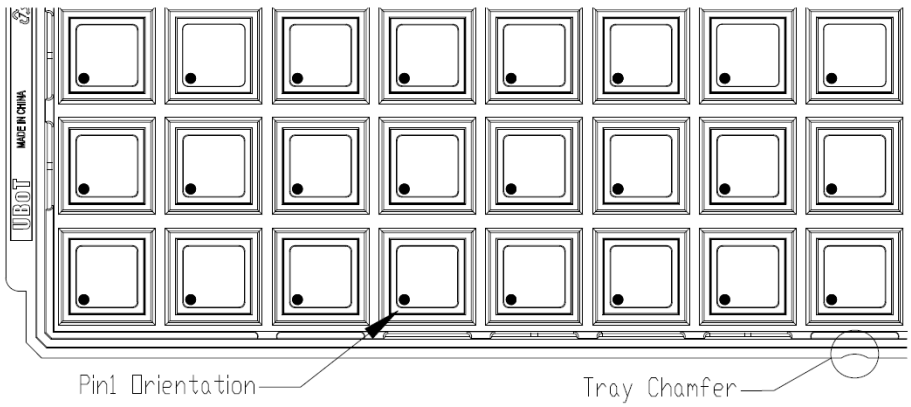
All photos are for reference only, and the appearance is subject to the product.

Table 53 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
G32A1445UAT0MLHR	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
G32A1445UAT0MLFR	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1

9.2 Tray packaging

Figure 34 Tray Packaging Diagram



Tray Dimensions

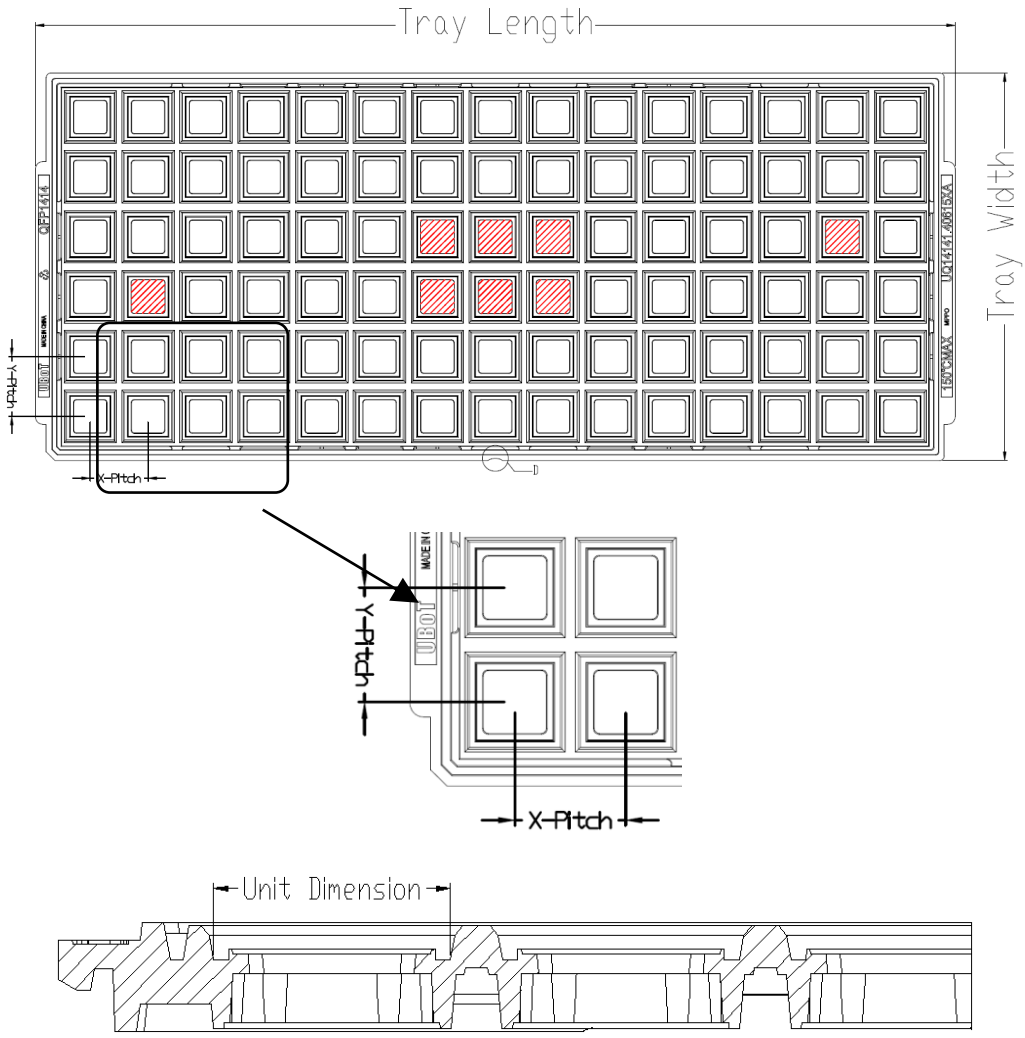


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Table 54 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
G32A1445UAT0MLLT	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32A1445UAT0MLHT	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32A1445UAT0MLFT	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9

10 Ordering Information

Figure 35 Product Information Naming Rules

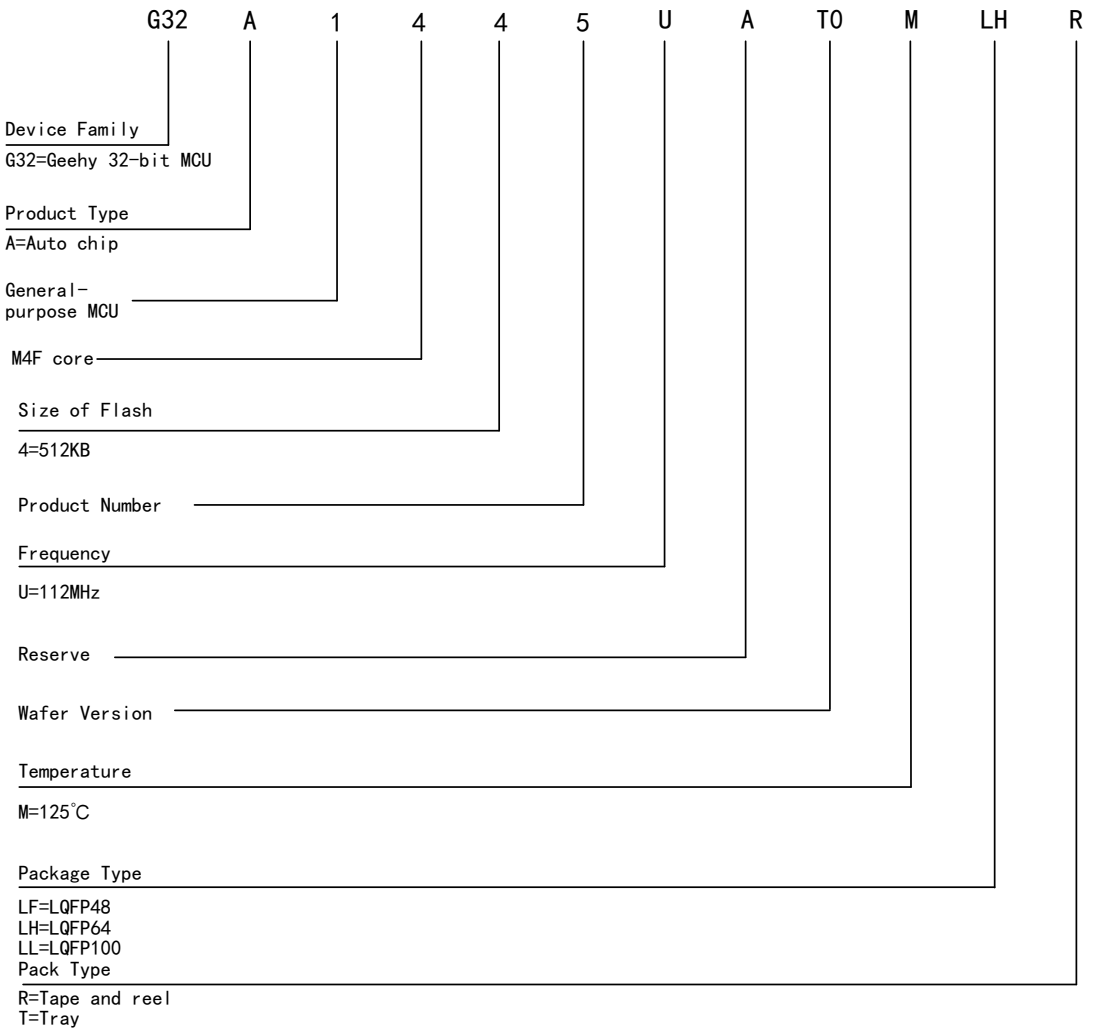

Table 55 Ordering Information Table

Order Code	Dominant frequency	Flash(KB)	SRAM(KB)	EEPROM(KB)	Package	SPQ	Temperature range
G32A1445UAT0MLFT	112MHz	512	64	4	LQFP48	2500	-40℃~125℃
G32A1445UAT0MLFR	112MHz	512	64	4	LQFP48	2000	-40℃~125℃
G32A1445UAT0MLHT	112MHz	512	64	4	LQFP64	1600	-40℃~125℃
G32A1445UAT0MLHR	112MHz	512	64	4	LQFP64	1000	-40℃~125℃
G32A1445UAT0MLLT	112MHz	512	64	4	LQFP100	900	-40℃~125℃

Note: SPQ = Smallest Packaging Quantity.

11 Commonly Used Function Module Denomination

Table 56 Commonly Used Function Module Denomination

Full name	Abbreviation
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External Interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C Interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC
Secure digital input/output	SDIO
Digital camera interface	DCI

12 Revision History

Table 57 Document Revision History

Date	Version	Revision History
November 2023	1.0	Initial Release
March 2024	1.2	● Delect G32A1445UAT0MLLR, G32A1445HAT0MLLR, G32A1445UAT0VLLR, G32A1445HAT0VLLR ● Modify Table Pin Multiplexing ● Modify the figure of LQFP Top View
June 2024	1.3	● Modify the descriptions of certain modules ● Modify the DAC module ● Modify the electrical characteristics of certain modules
August 2024	1.4	● Modify product features, product information, and pin functions
October 2024	1.5	● Add flash storage time and erase cycle
March 2025	1.6	● Increase LQFP48 encapsulation ● Modify write durability and cycle durability
July 2025	1.7	● Modify the power consumption data for 64MHz
August, 2025	1.8	● Delete some order codes
September, 2025	1.9	● Modify Product Characteristics Chapter
November, 2025	2.0	● Reformatted Table 5 Pin Multiplexing
March 2026	2.1	● Update Figure 32

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